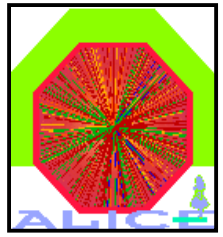


Commissioning di SDD con il run di raggi cosmici

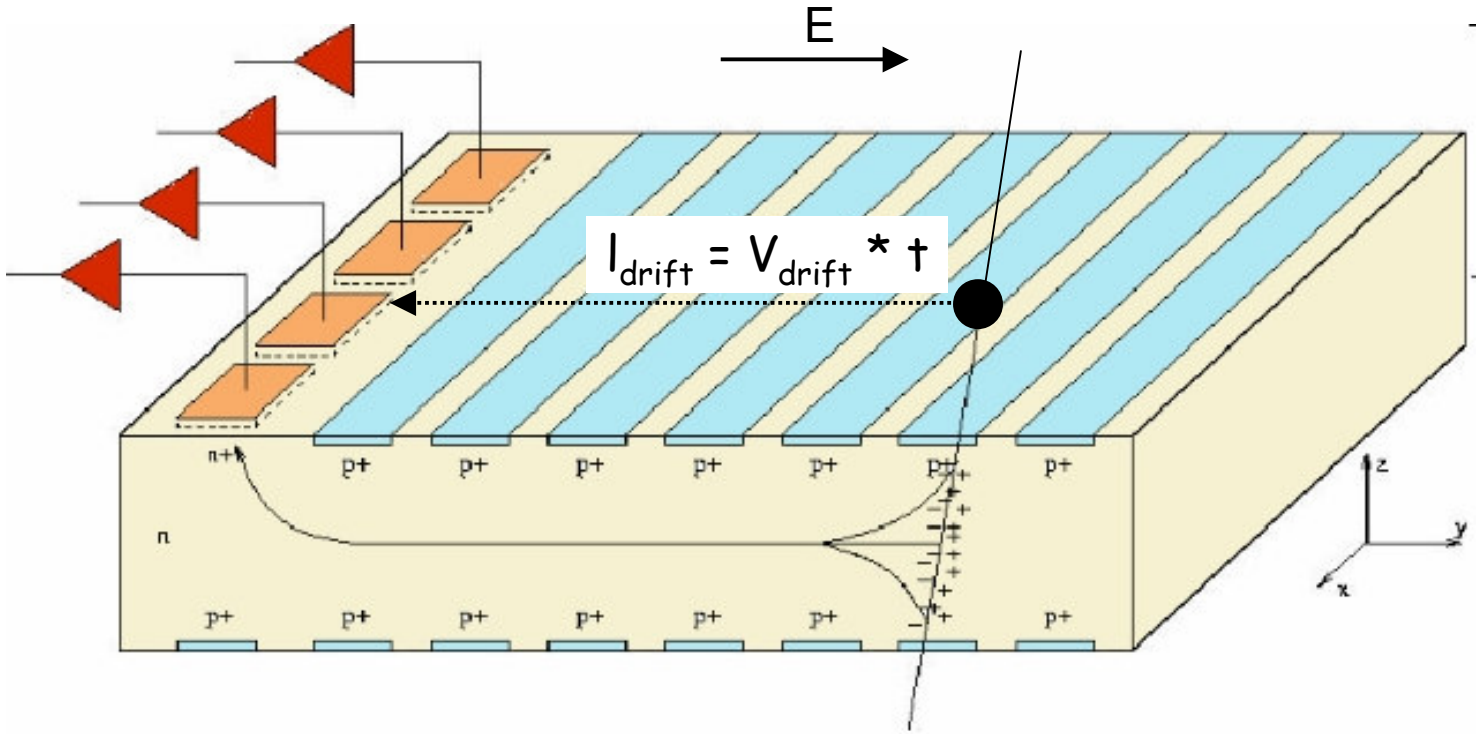
Davide Falchieri
Università e INFN, Bologna

Quinto convegno nazionale sulla fisica di ALICE, Trieste 2009

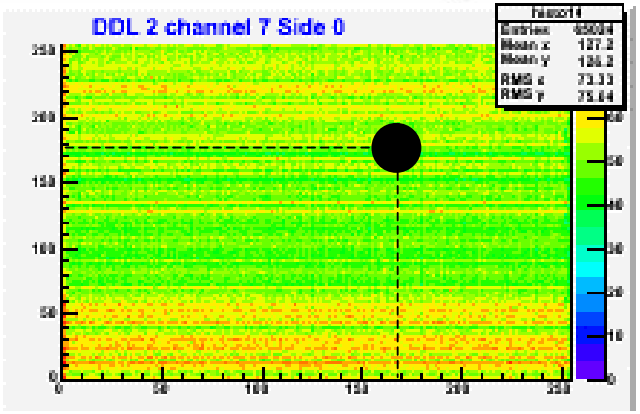
Outline

- Il rivelatore SDD
- La catena di acquisizione dati di SDD
- Formato dati
- Calibrazione del rivelatore:
  - ✓ *run di pedestal*
  - ✓ *run di testpulse*
  - ✓ *run di injector*
- Statistiche sul funzionamento e prestazioni
- Ricostruzione di tracce di raggi cosmici
- Ottimizzazione del SOP delay
- Conclusioni

Il rivelatore SDD

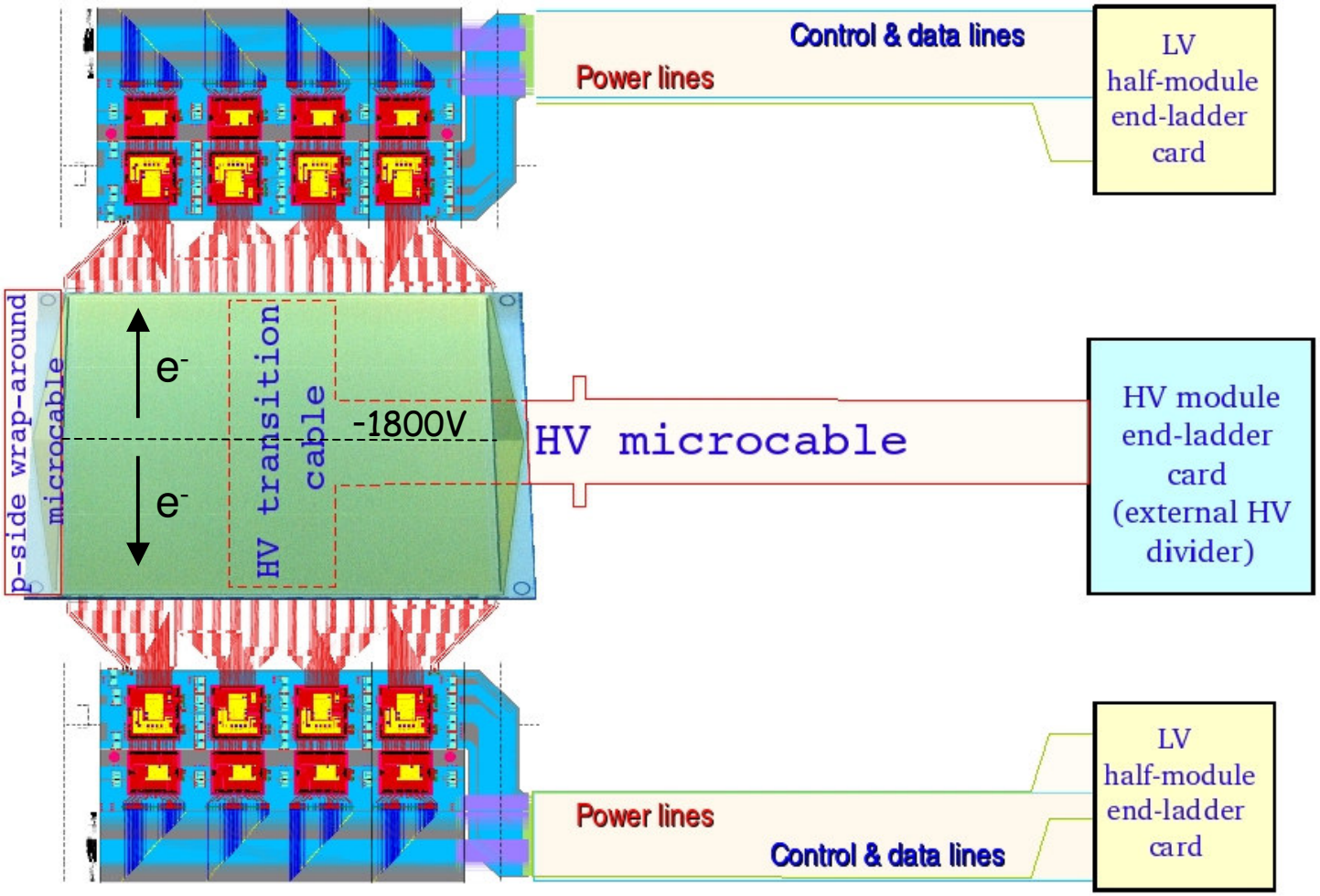


anodi



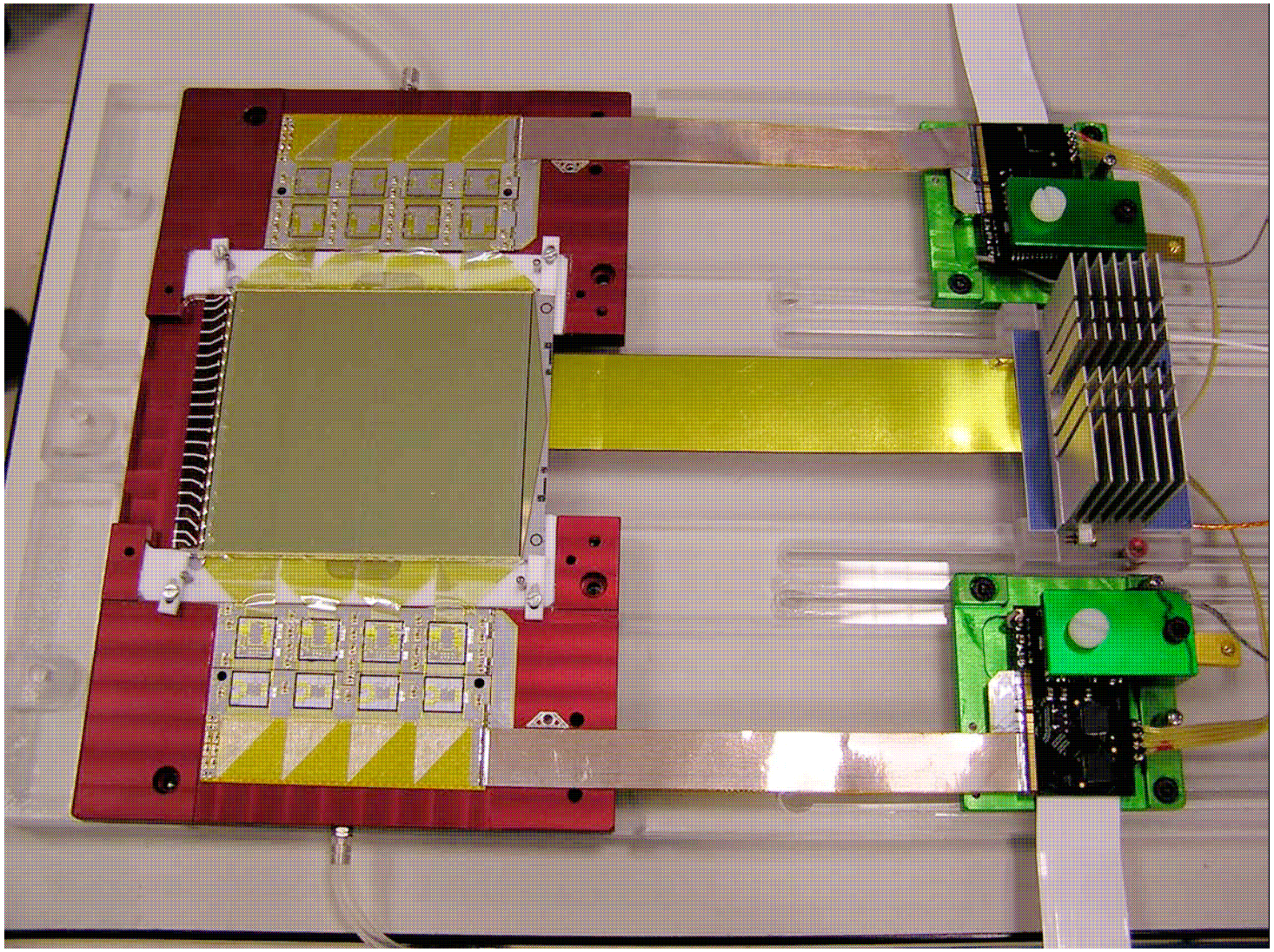
time bin

Modulo SDD

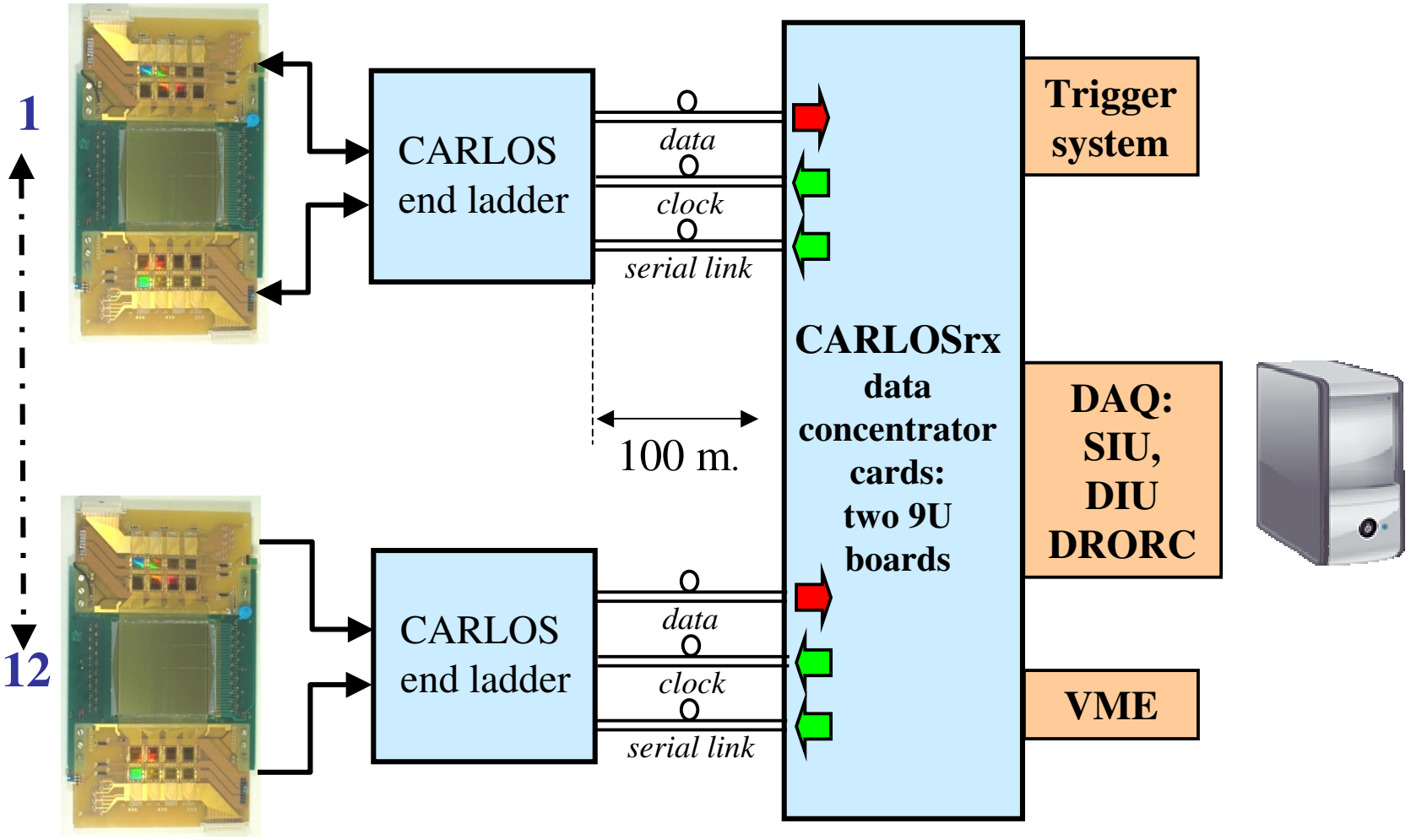


FEE (4 coppie di ASIC)
-> PASCAL
-> AMBRA

Modulo SDD



Layer	# ladder	mod/ladder	# moduli
3	14	6	84
4	22	8	176



260 rivelatori SDD

24 schede CARLOSrx

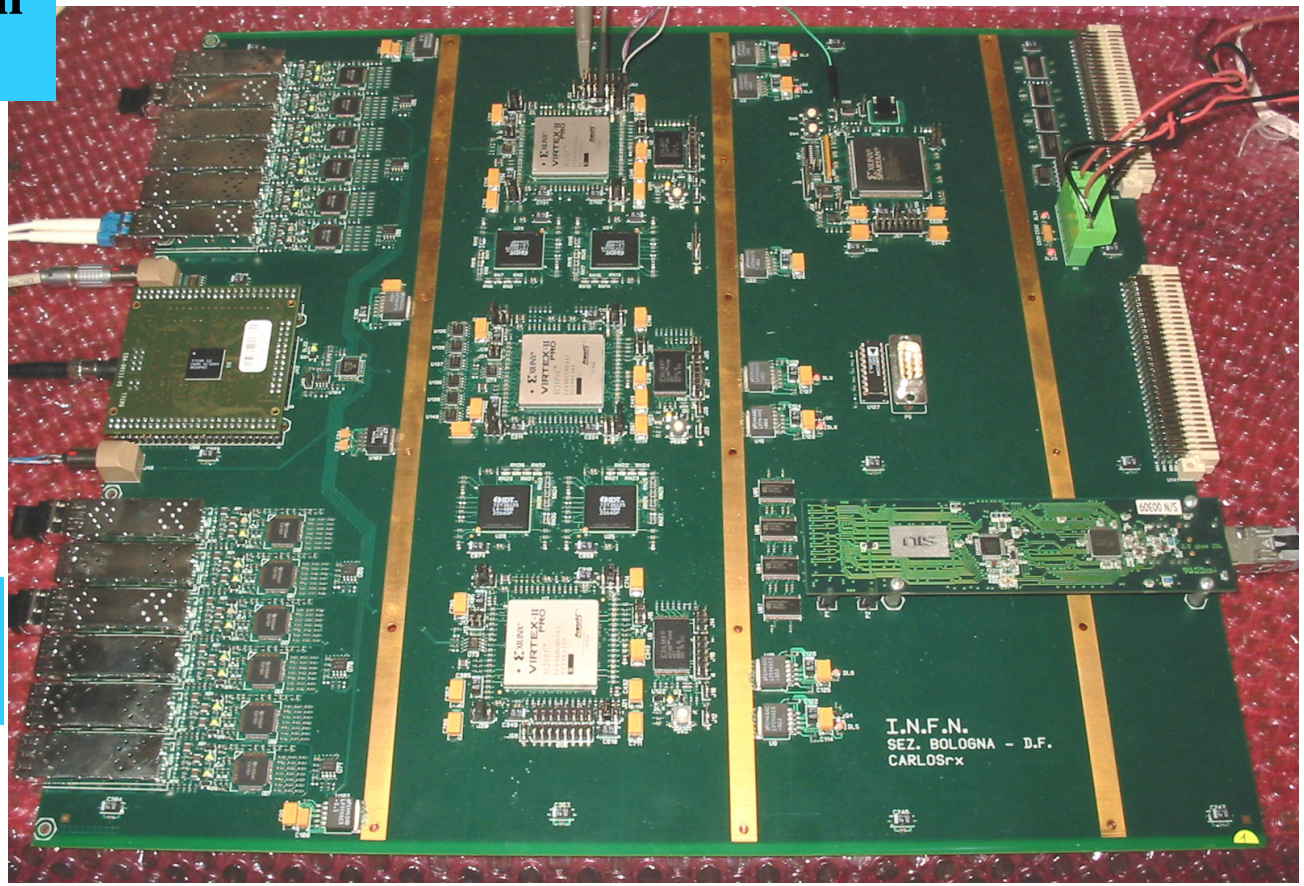
Scheda di readout CARLOSrx

6 moduli SDD

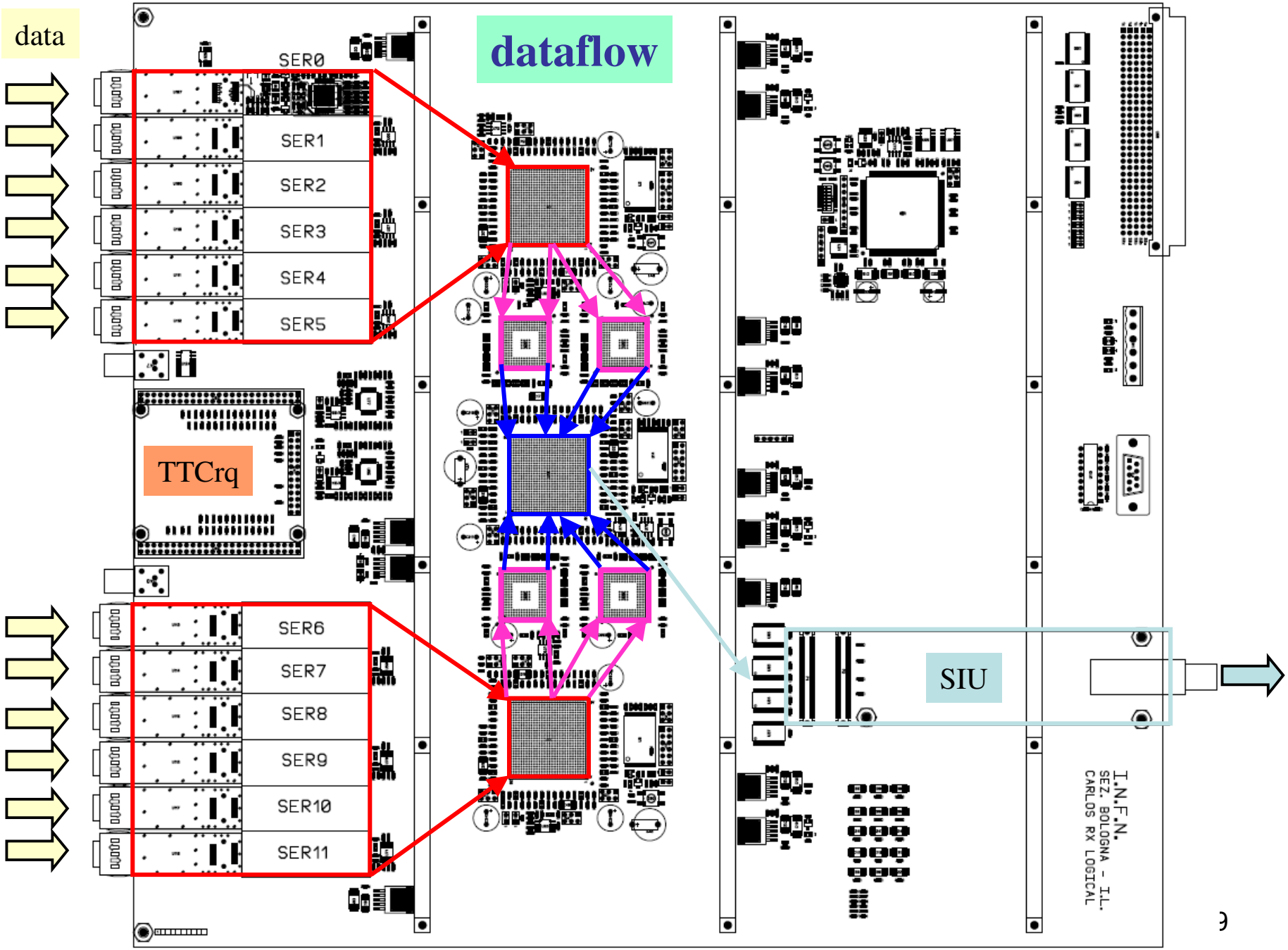
busy

TTCrq

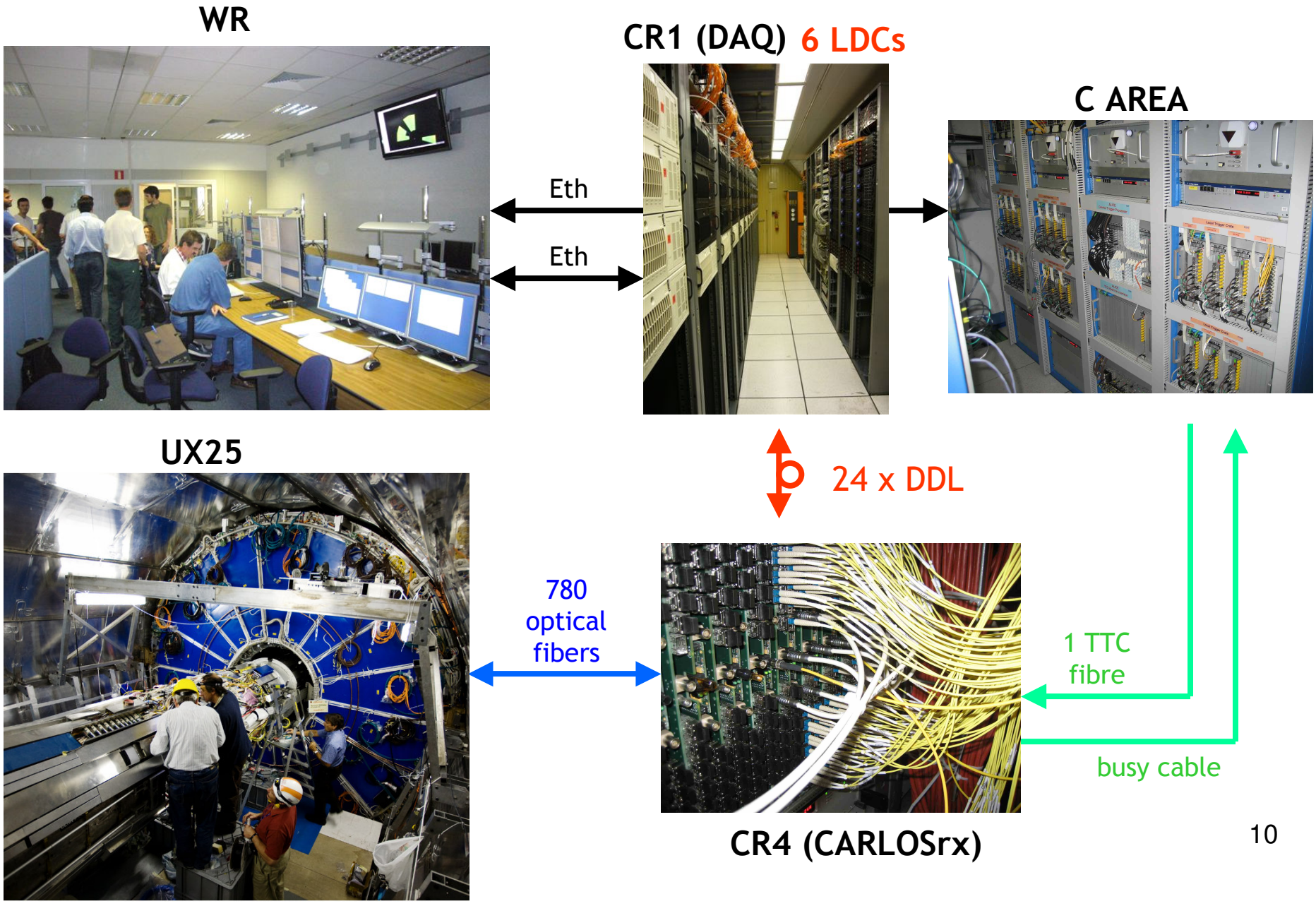
6 moduli SDD



DDL


data
dataflow
SER0
SER1
SER2
SER3
SER4
SER5
TTCrq
SER6
SER7
SER8
SER9
SER10
SER11
SIU
I.N.F.N.
SEZ. BOLOGNA - I.L.
CARLOS RX LOGICAL

Commissioning of the SDD



Dimensione degli eventi

Formato dati 2008

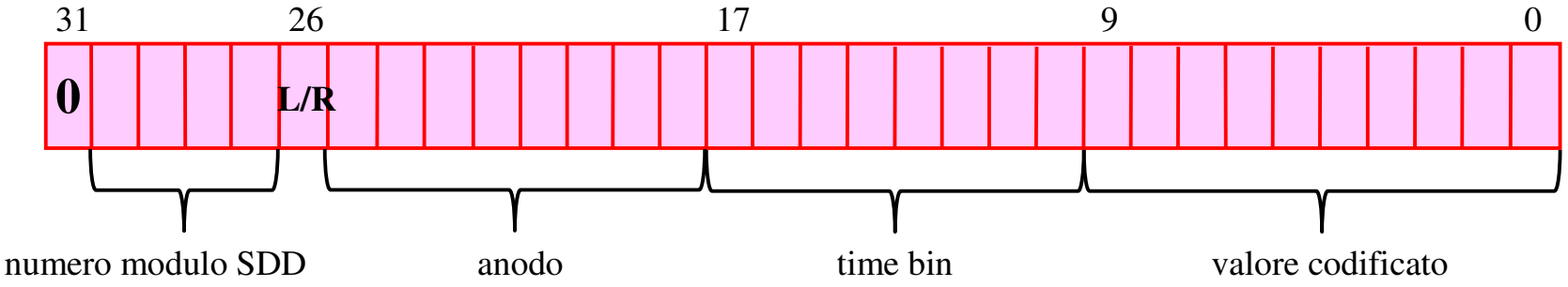
- Dimensione di un evento vuoto:
  - ⇨Header + Footer (6 parole da 32 bit x Nmoduli): 6 kB/evento
  - ⇨End Of Row Summary (21 bit x 512 anodi x Nmoduli): 350 kB/evento
  - ⇨Parole di identificazione canali dati: 160 kB/evento
  - ⇨**Total:** **516 kB/evento**

- Ciò significa 516 MByte/s con un event rate di 1 KHz

- Era quindi necessario:
  - ⇨ Ridurre il volume dati di almeno un fattore 20

Nuovo formato dati

- Soluzione proposta:
  - ⇨1 parola da 32 bit per ogni cella accesa (anodo/time bin)
  - ⇨1 parola di controllo (32 bit) alla fine di ogni modulo
  - ⇨1 parola di jitter (32 bit) alla fine di ogni evento

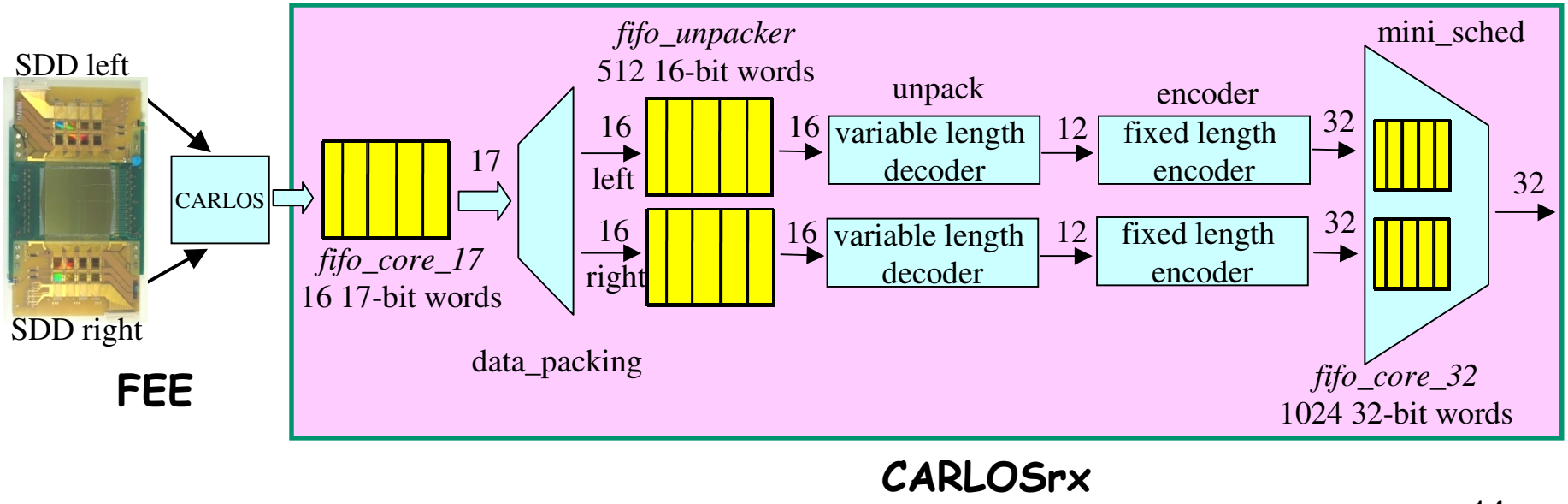


- Dimensione di un evento "vuoto":
  - ⇨DATI: 4 Byte * numero di celle accese (≈ 4000)
  - ⇨CONTROL: 4 Byte * 260 (numero di moduli SDD)
  - ⇨JITTER: 4 Byte * 24 (numero di schede CARLOSrx)
  - ⇨**Total: ≈ 17 kByte/evento**

Nuovo formato dati

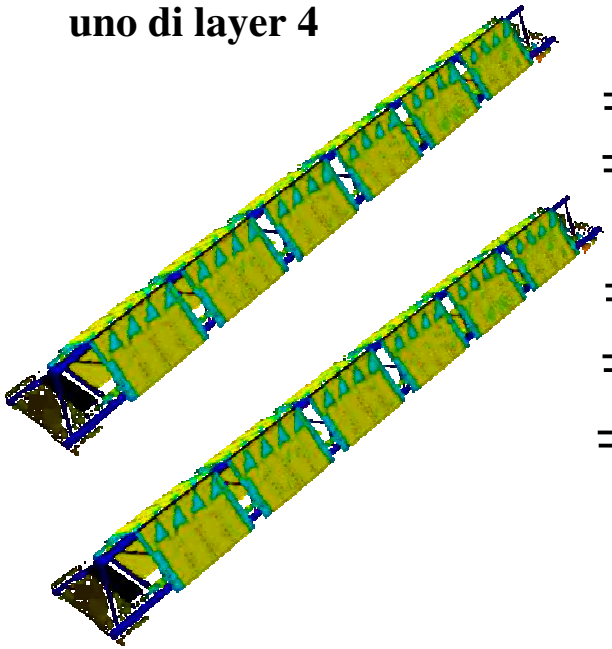
Sono state provate due soluzioni:

- ⇨ Soluzione software sui PC dell'HLT:
  - ✓ ***Provato in Settembre 2008 al CERN***
  - ✓ ***OK, ma limitato ad un massimo event rate di 400 Hz***
- ⇨ Soluzione hardware: nuovo firmware sulle FPGA delle CARLOSrx
  - ✓ ***Sviluppato nell'Inverno 2008/09 a Bologna***

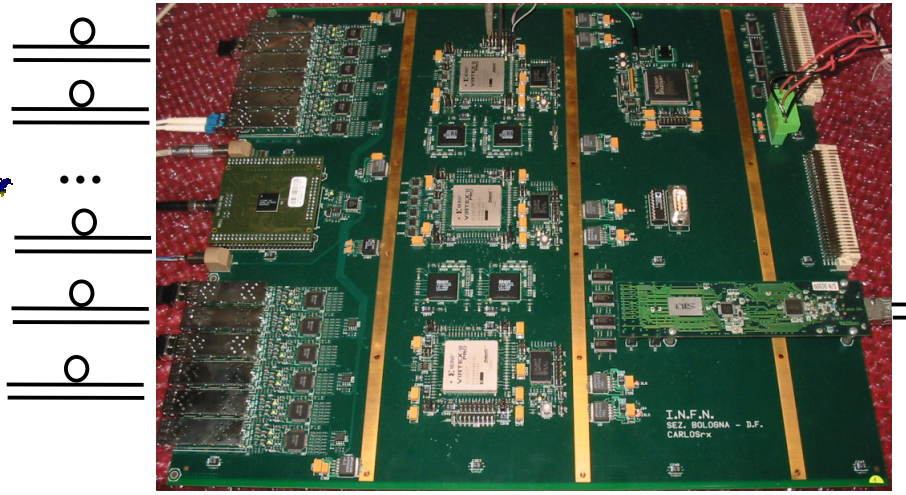


SDD setup a Bologna

2 ladder SDD :
uno di layer 3
uno di layer 4



12x3 fibre ottiche

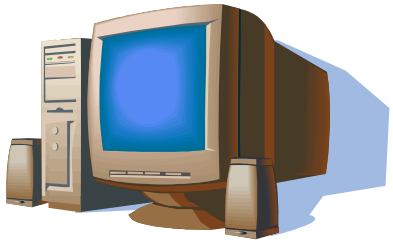


CARLOSrx

trigger PC

DAQ PC

LV + MV + HV
alimentazione

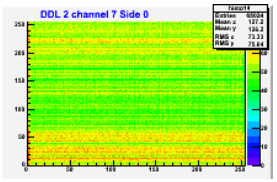


DCS PC

Prestazioni dell'implementazione hardware (128 campioni per anodo, AM @ 20 MHz, ADC @ 40 MHz)

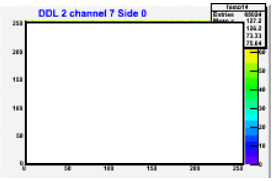
	Event size (MByte)	Max rate (Hz)
1 modulo	0.25	380
2 moduli	0.5	290
4 moduli	1	150
6 moduli	1.5	108
8 moduli	2	80
10 moduli	2.5	64

compressione non attiva



	Event size (Byte)	Max rate (Hz)
1 modulo	140	990
2 moduli	144	990
4 moduli	152	990
6 moduli	160	990
8 moduli	168	990
10 moduli	176	990

compressione attiva



Run di calibrazione

(info da Francesco Prino)

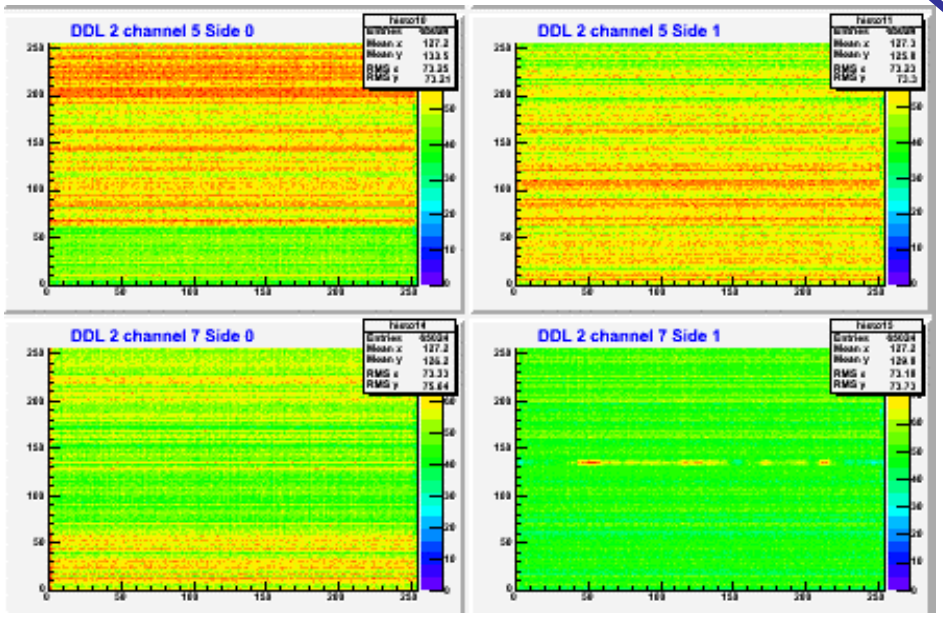
Tipi di run per SDD

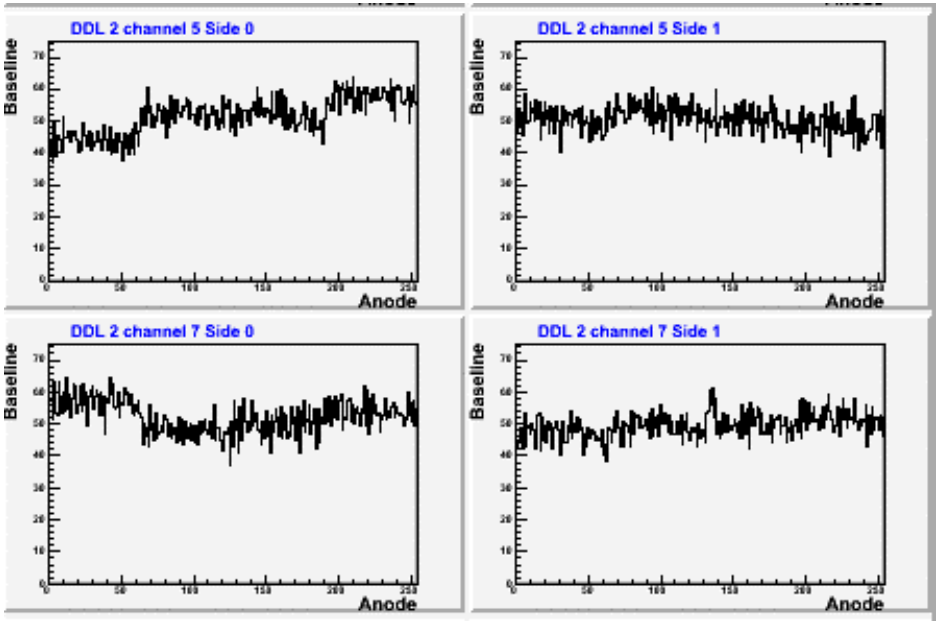
- STANDALONE
  - ⇨Run di controllo
- PEDESTAL
  - ⇨Per misurare **baseline** e **noise**
  - ⇨Senza compressione 2D e senza equalizzazione di baseline
- PULSER
  - ⇨Per misurare **il guadagno** da testpulse
  - ⇨Senza compressione 2D e senza equalizzazione di baseline
- INJECTOR
  - ⇨Per misurare **la velocità di deriva** dagli iniettori
  - ⇨Compressione 2D ed equalizzazione di baseline attive

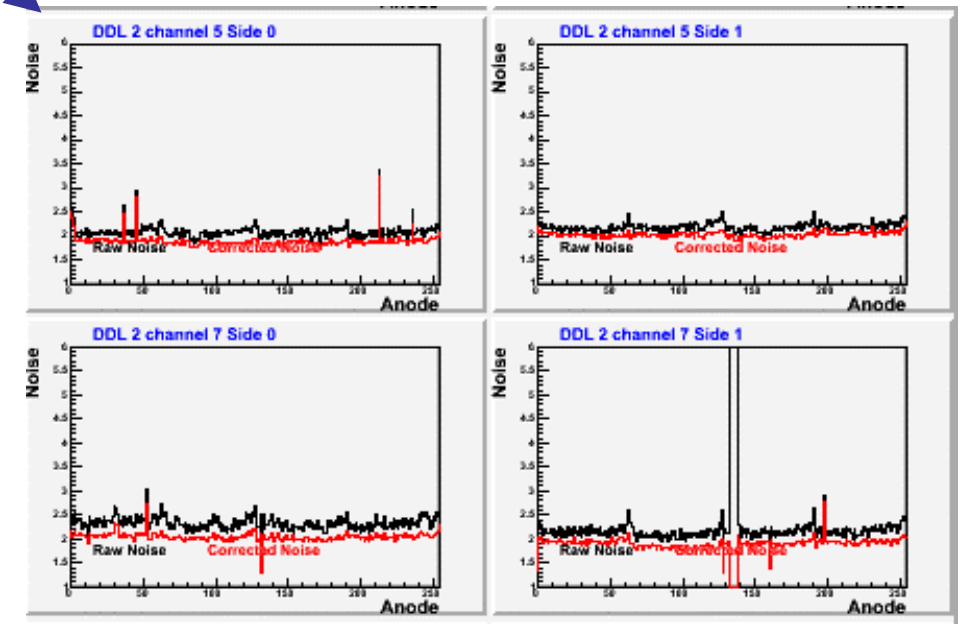
Pedestal run

- baseline
- noise (**con** e **senza** correzione di common mode)

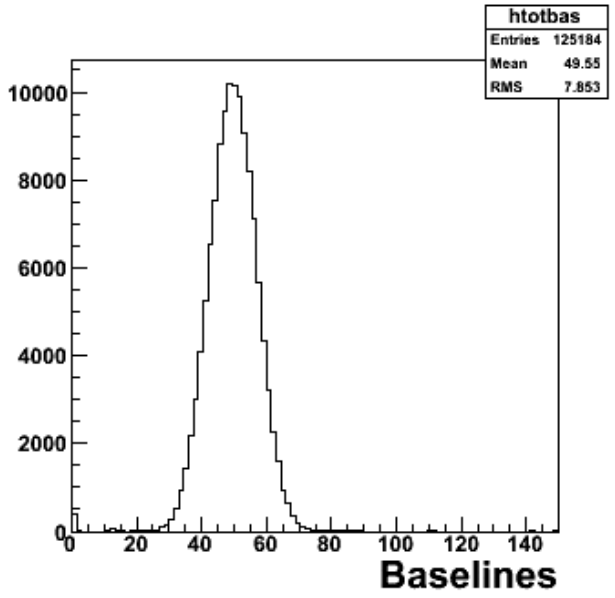
per ogni anodo

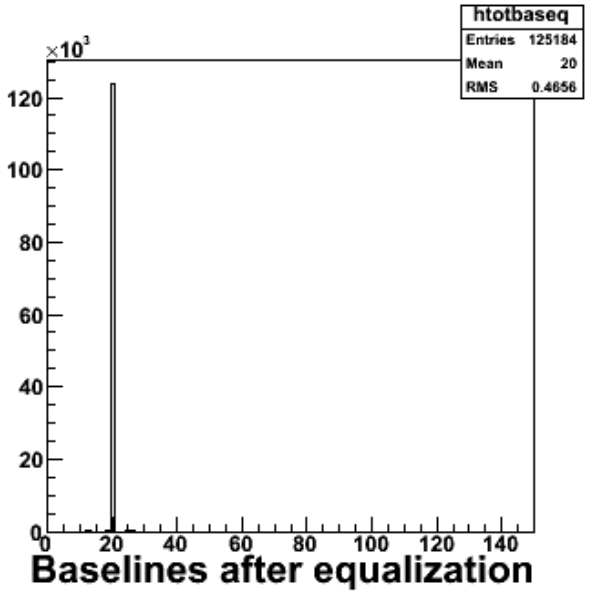


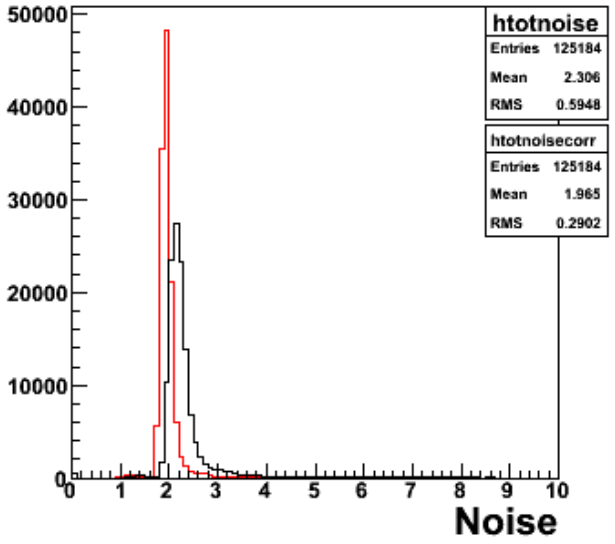


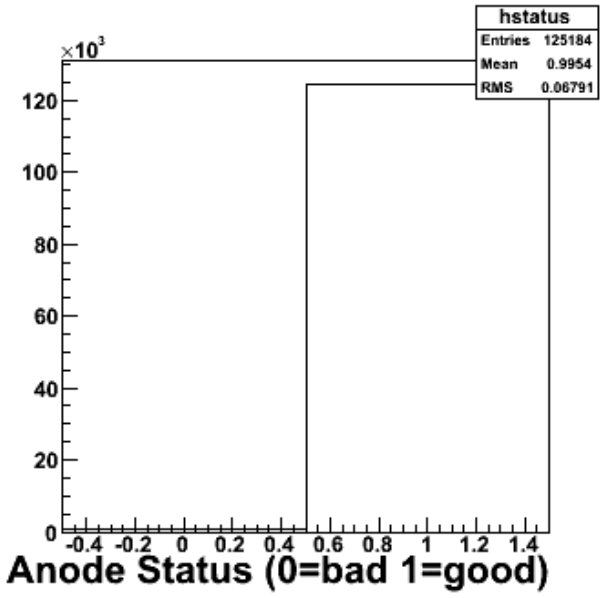


Pedestal: statistiche sugli anodi

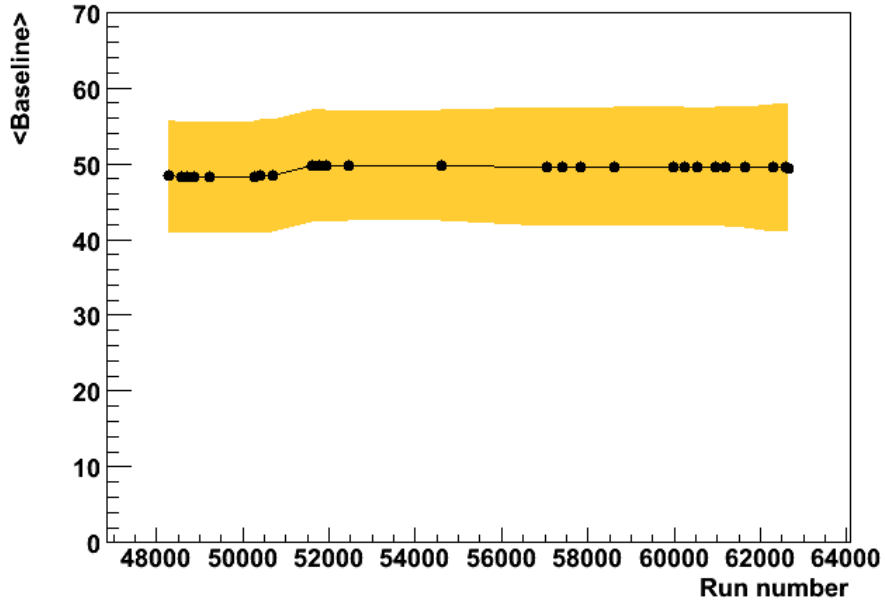


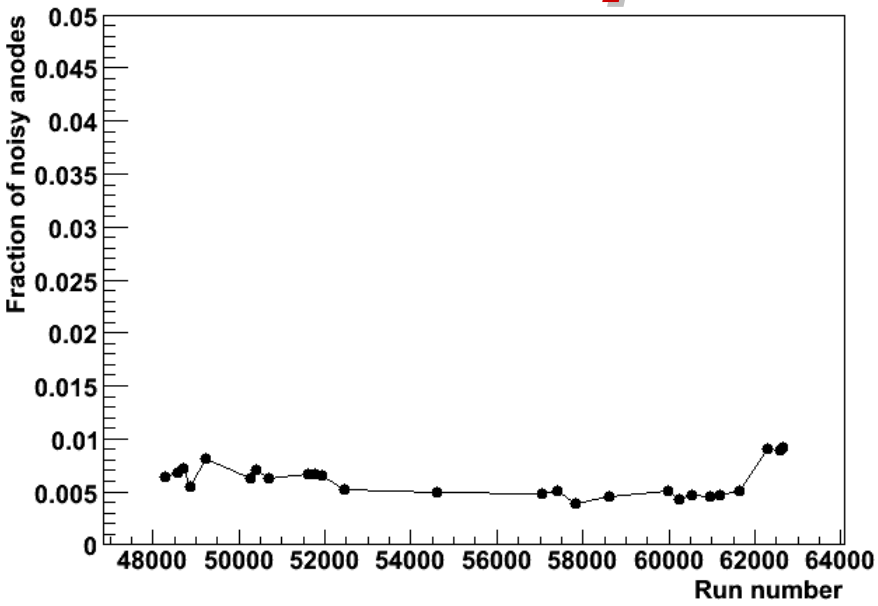


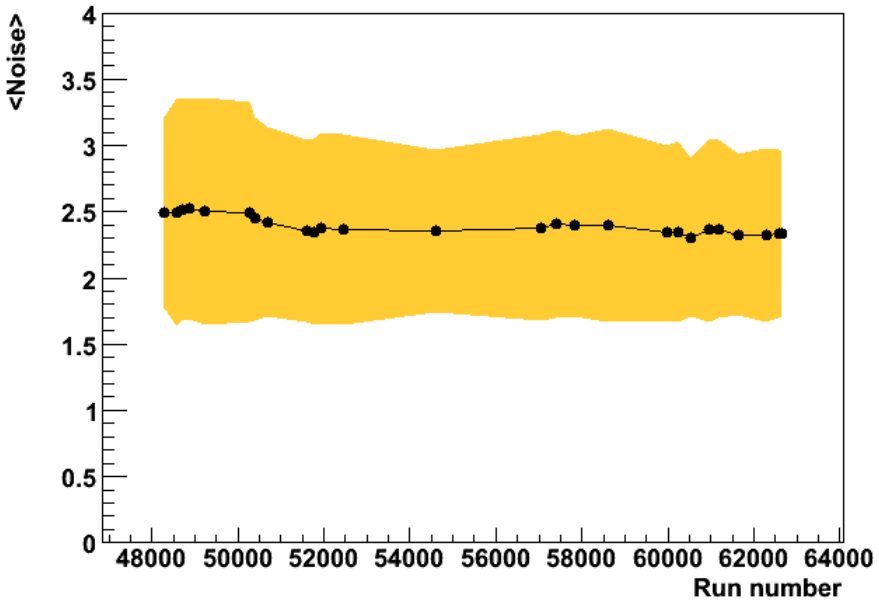


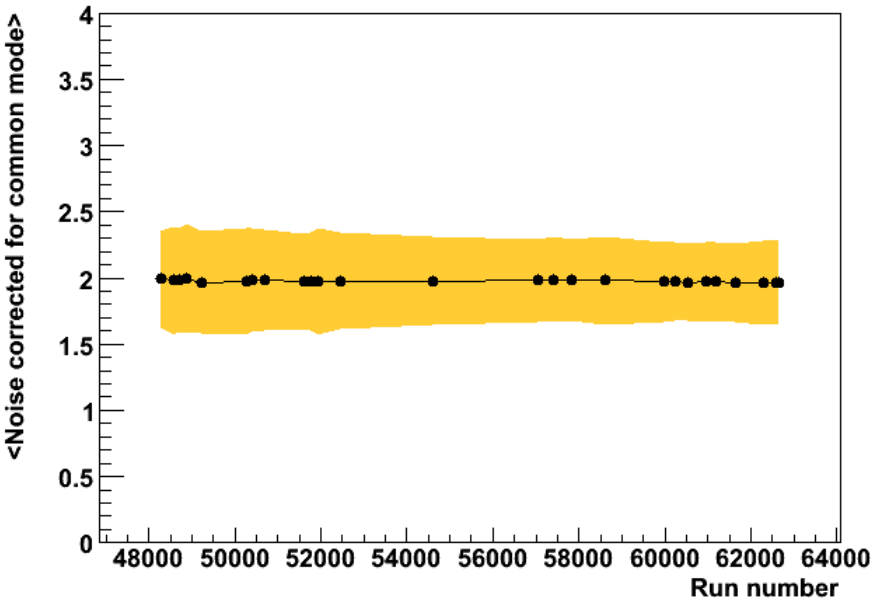


Pedestal: stabilità nel tempo

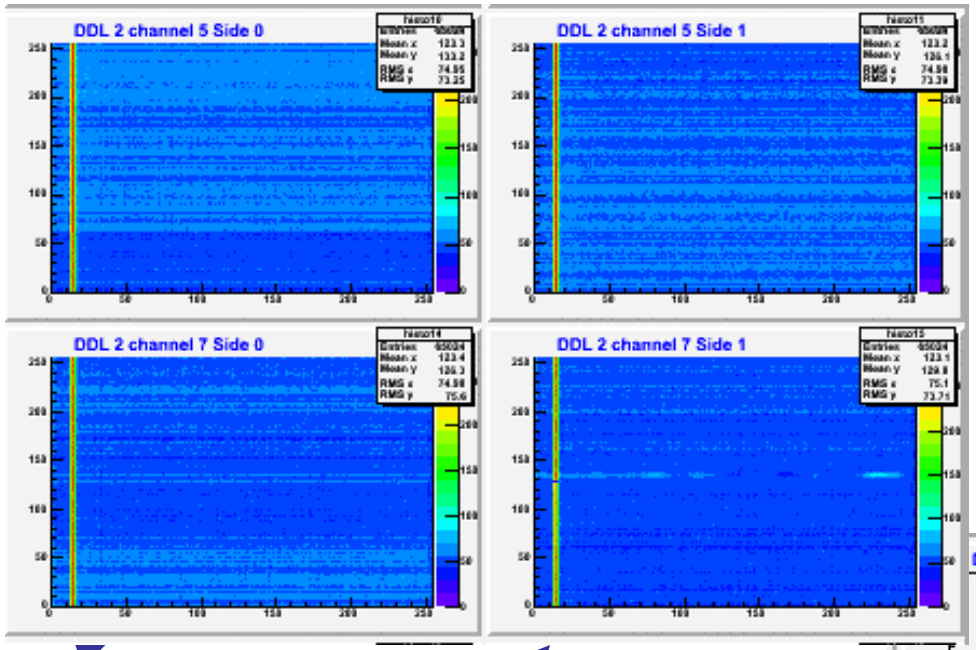


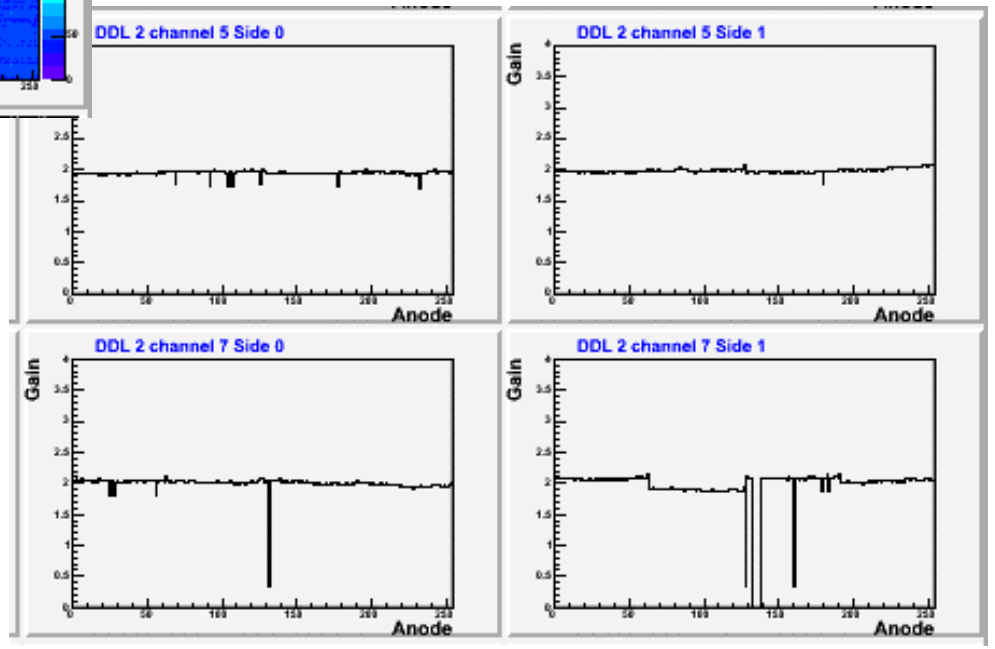






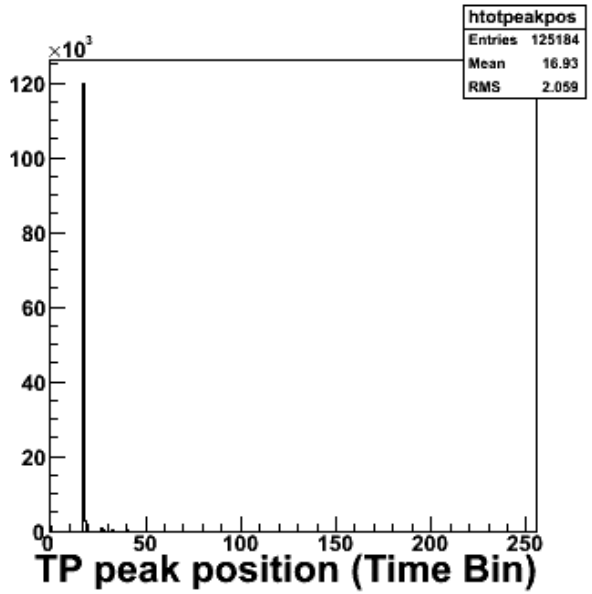
Pulser run

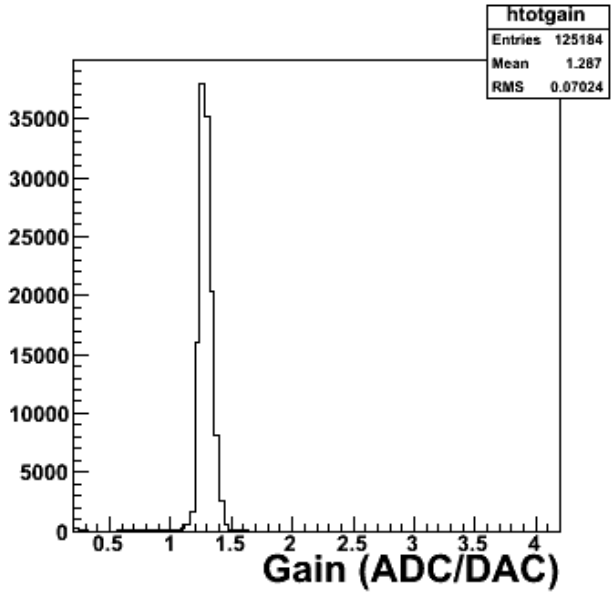


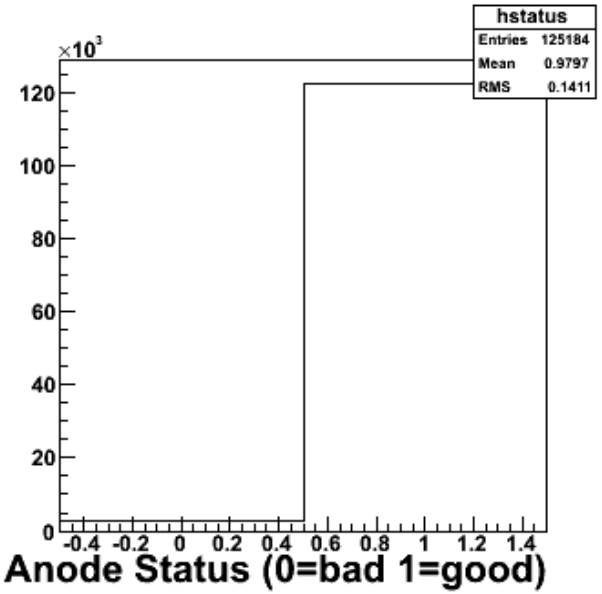


Segnale di Testpulse

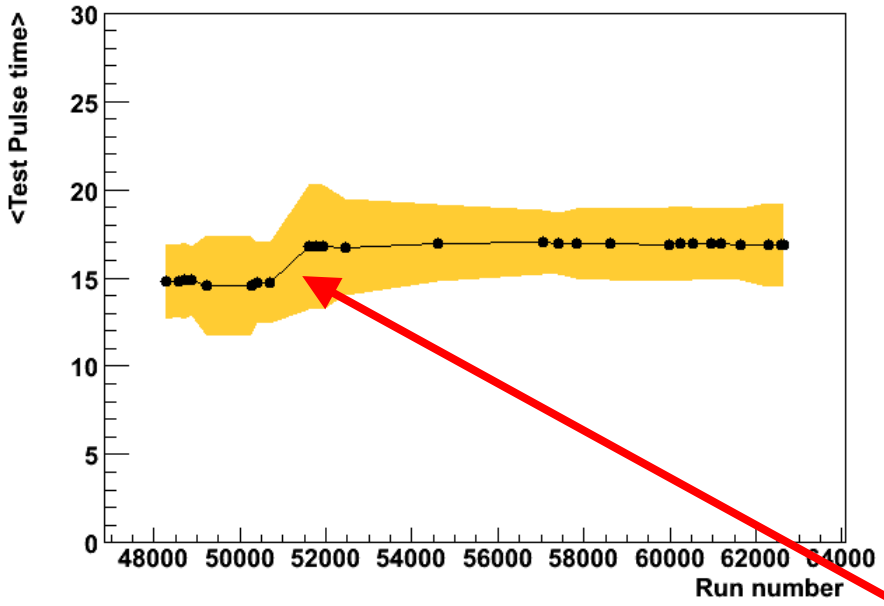
Pulser: statistiche sugli anodi

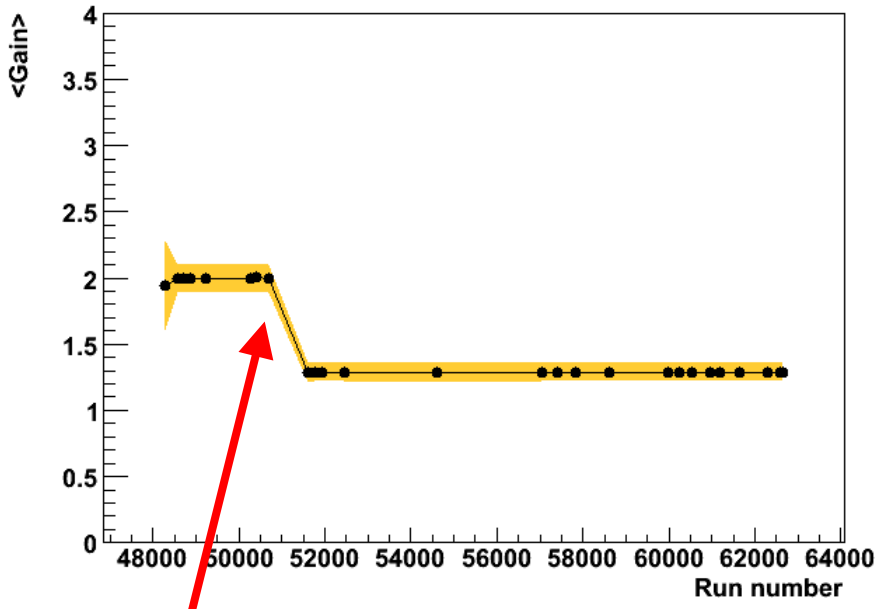


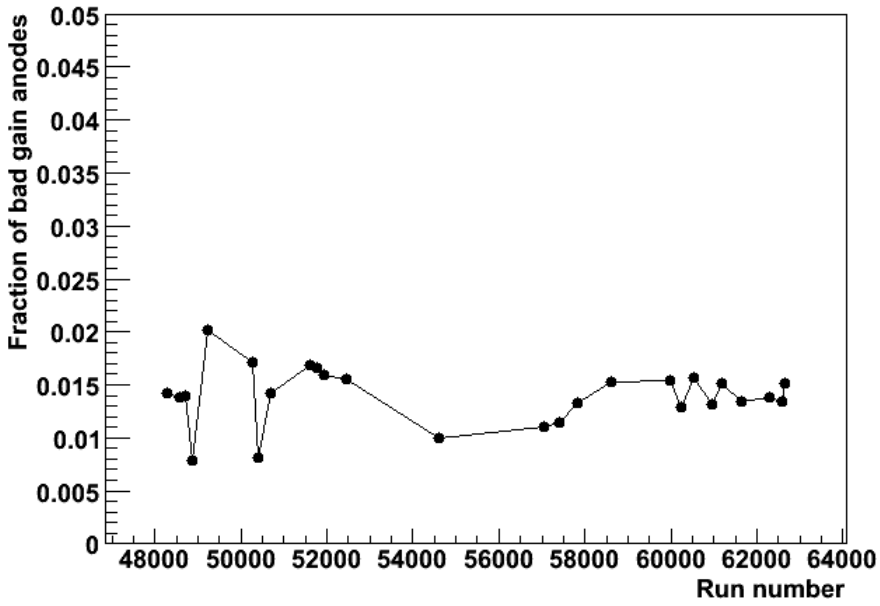




Pulser: stabilità nel tempo



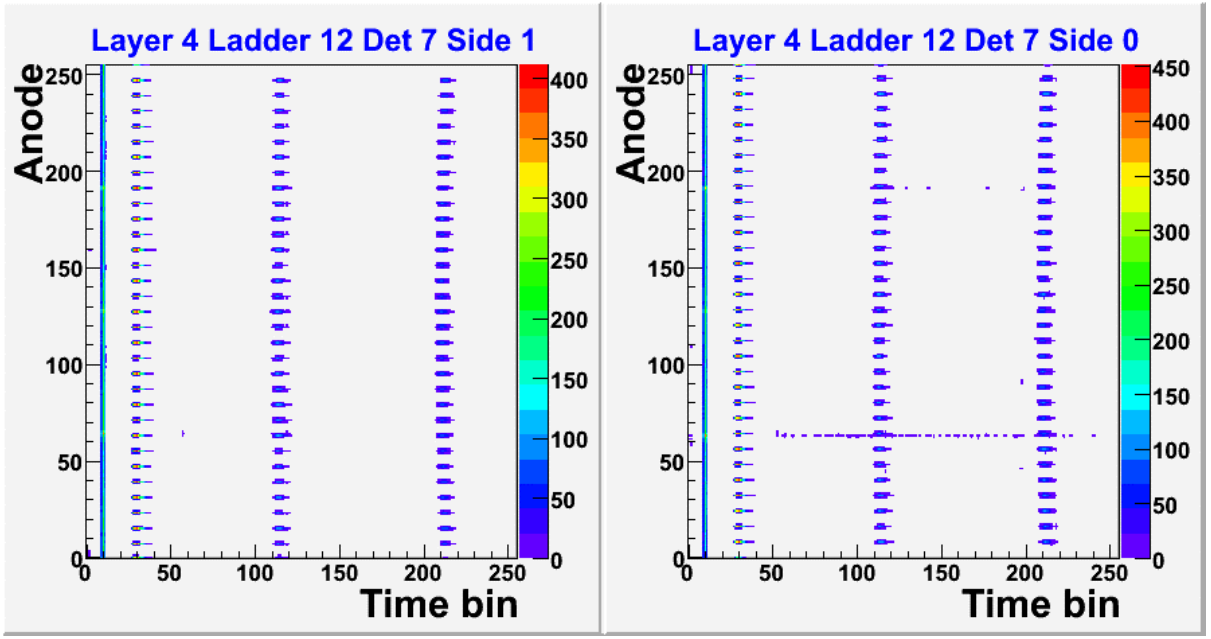


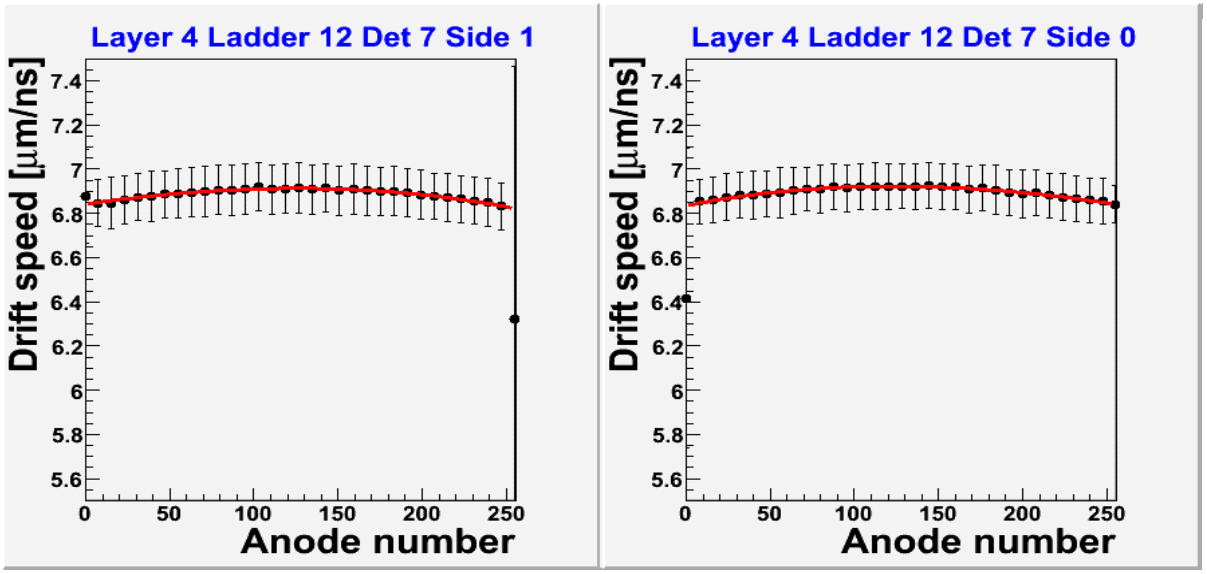


passaggio della frequenza della memoria analogica di PASCAL da 40 MHz a 20 MHz

Injector run

- 33 (1 ogni 8 anodi) x 3 iniettori ogni $\frac{1}{2}$ SDD
- Velocità di deriva ricavata dal tempo di deriva misurato e dalla distanza di deriva nota

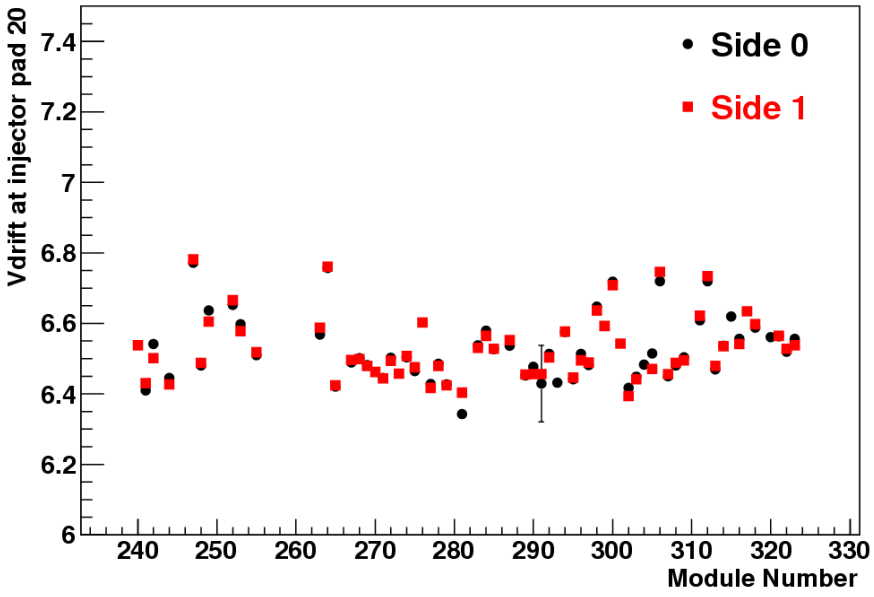




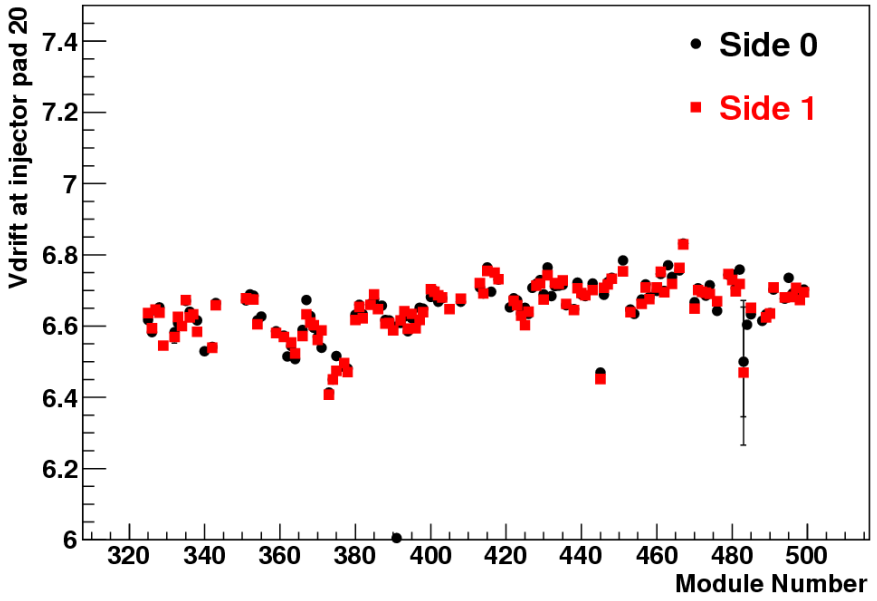
- La velocità di deriva dipende dall'anodo :
  - ⇨ Dipende dalla temperatura

    $v_{drift} = \mu_e E$, $\mu_e \propto T^{-2.4}$
  - ⇨ Le sorgenti di calore (voltage divider) stanno sui bordi

Velocità di deriva vs moduli



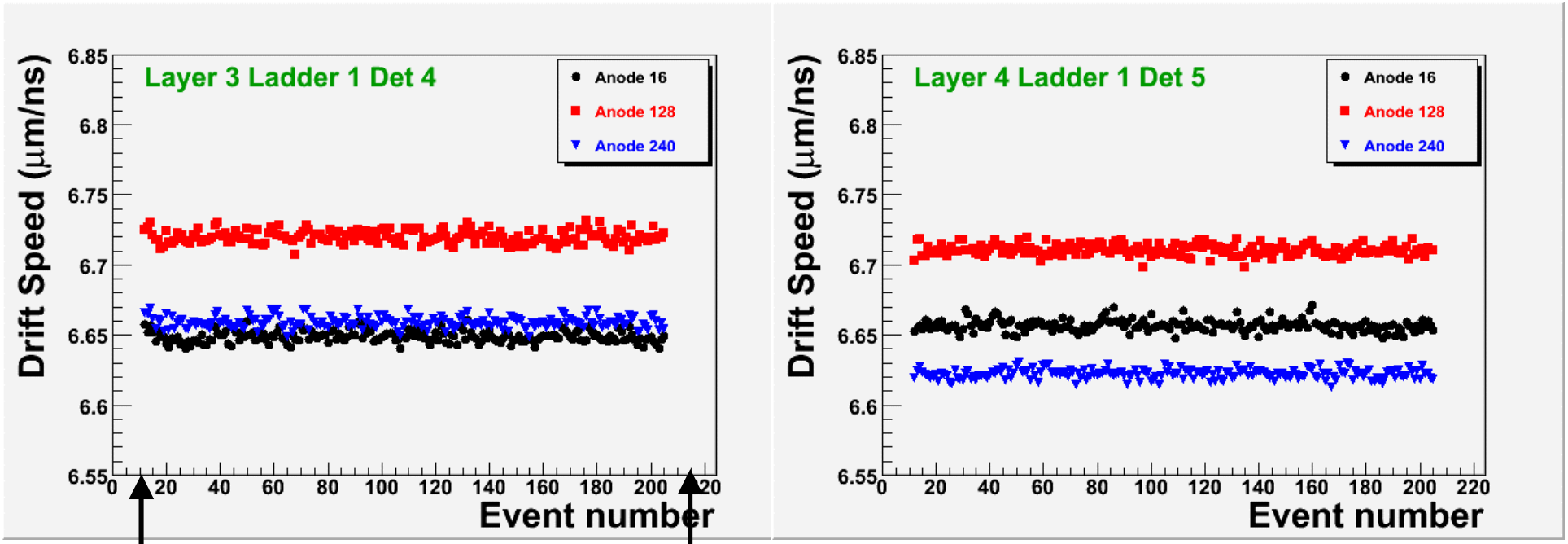
layer 3



layer 4

Stabilità della v_{drift}

- Dal run 24906:
  - ⇨ circa 5 trigger/minuto, 200 eventi analizzati
- v_{drift} è costante sulla scala di tempi di un'ora

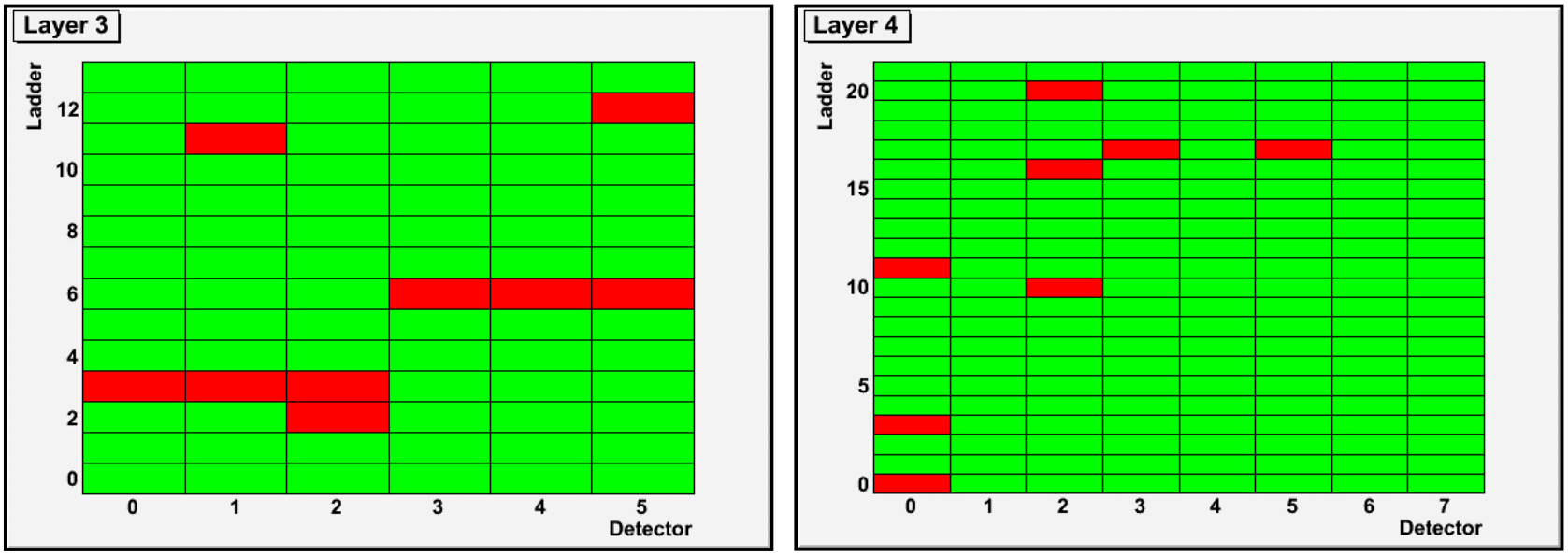


Timestamp=1204588292
Mon, 03 Mar 2008 23:51:32 GMT

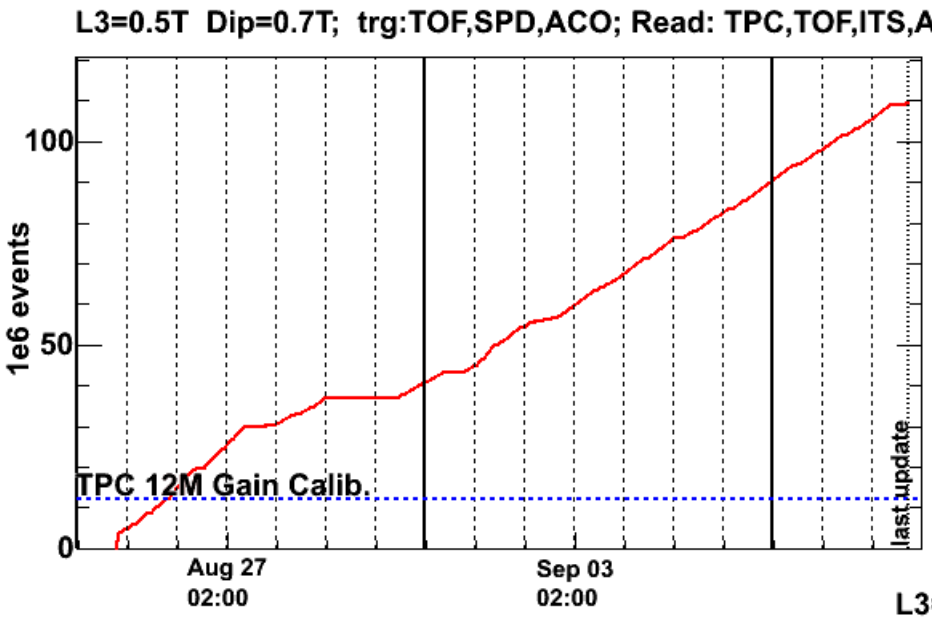
Timestamp=1204592726
Tue, 04 Mar 2008 01:05:26 GMT

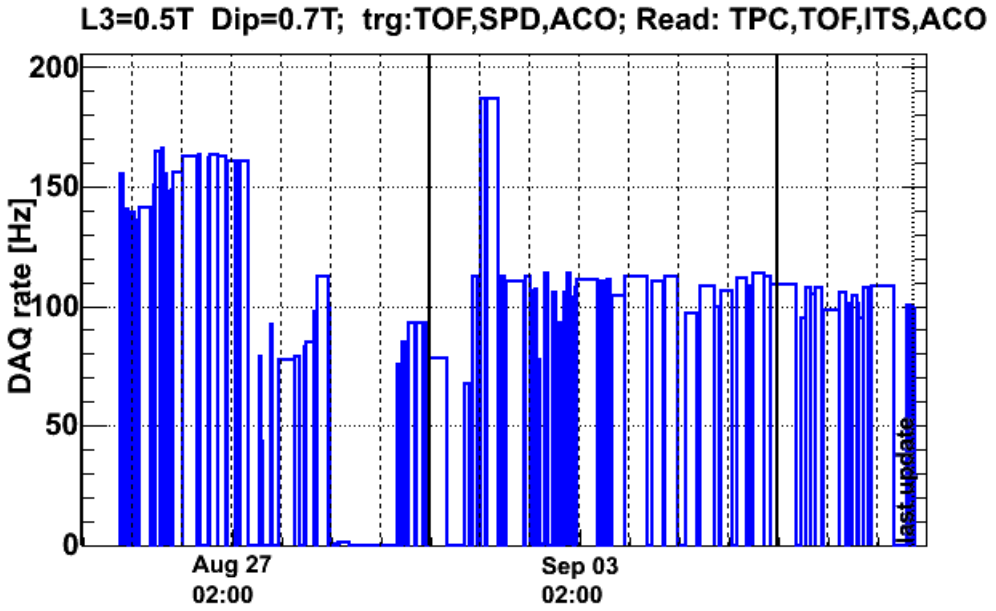
Statistiche run di raggi cosmici 2009

Numero di moduli in acquisizione:	247/260
Totale ore di run nella partizione PHYSICS:	> 100 h
Numero di eventi acquisiti:	> 100 M
Dimensione media di un evento SDD:	10 KByte
Event rate medio (trigger ACORDE+SPD+TOF)	110 Hz



Moduli SDD utilizzati per il run di raggi cosmici 2009



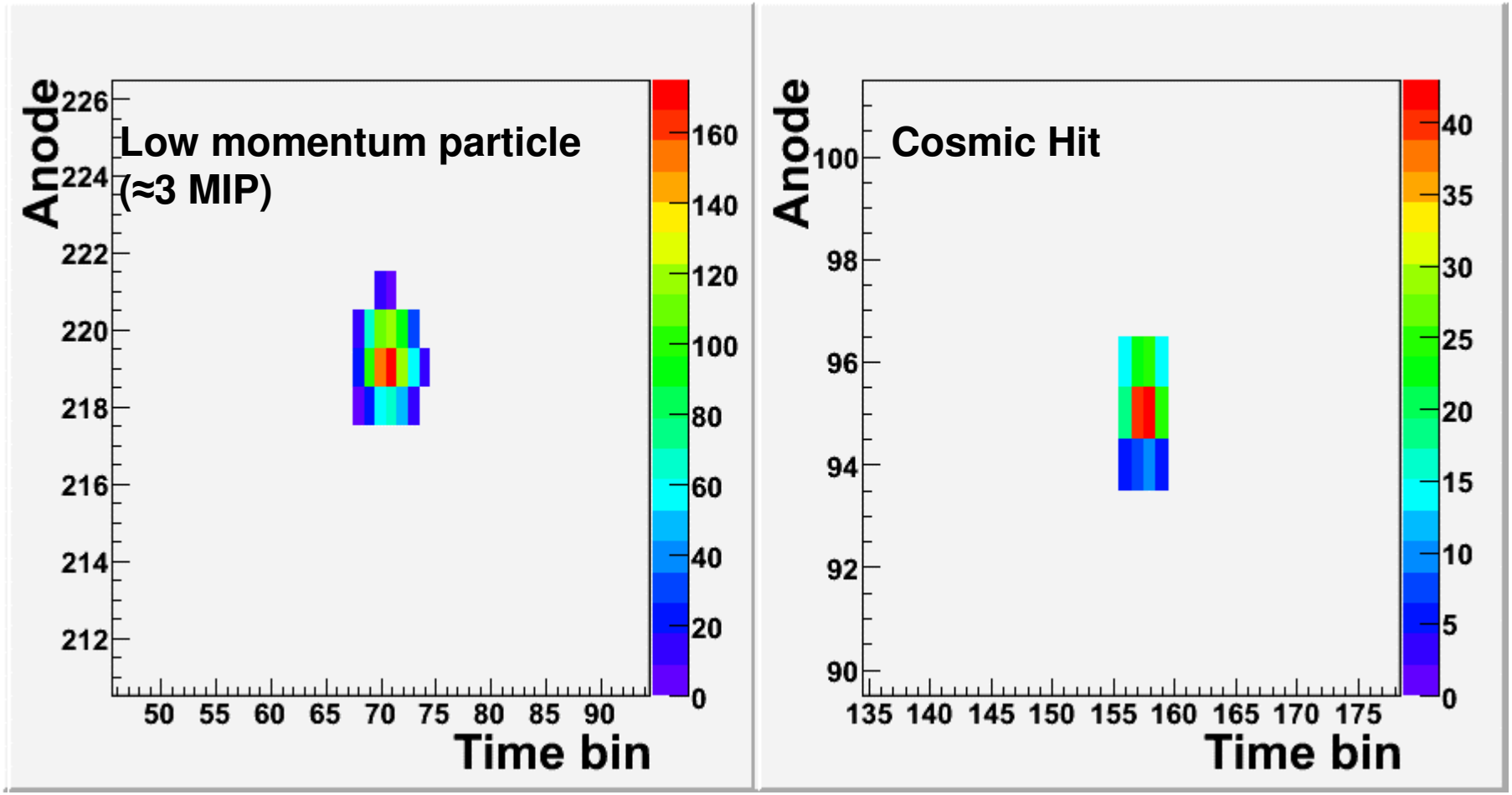


from: **http://aliceinfo.cern.ch/Collaboration/Run_Coordination/Run09/cosmics/**

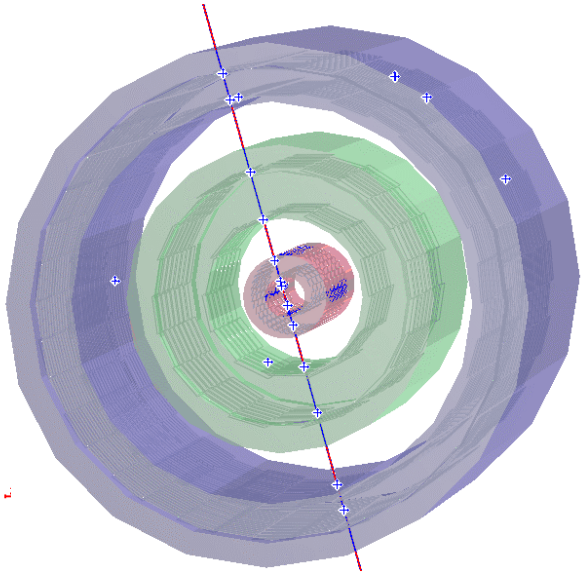
Ricostruzione di tracce di raggi cosmici

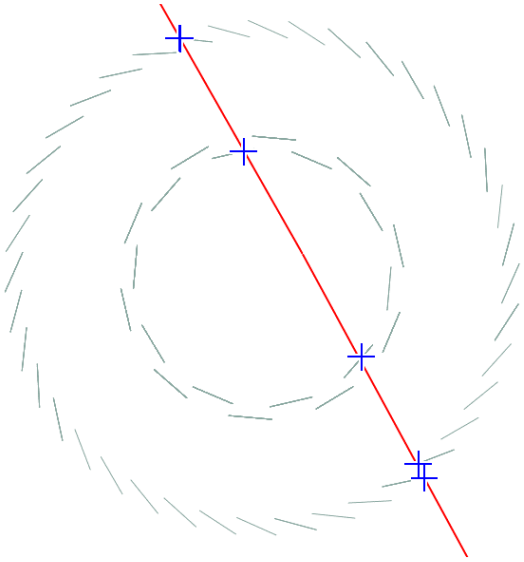
SDD hit

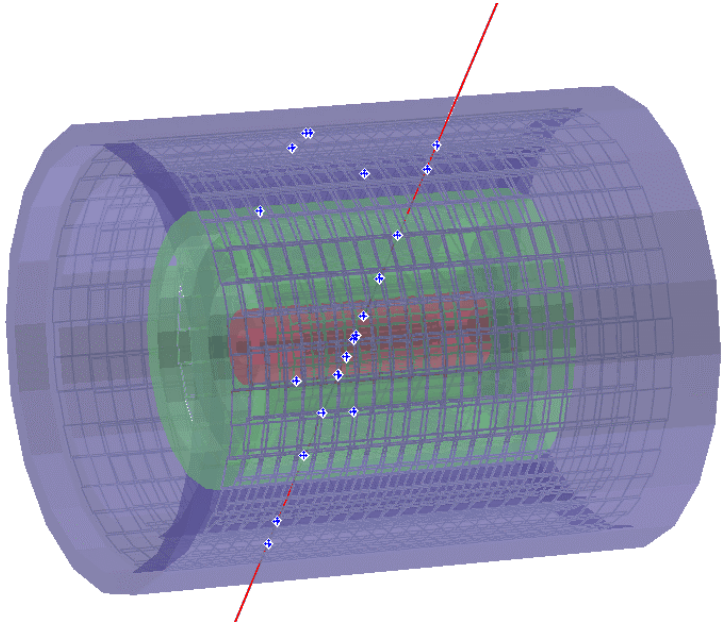
Run22252 012.2990 ev 31
Layer 4 – Ladder 9 – Det 4



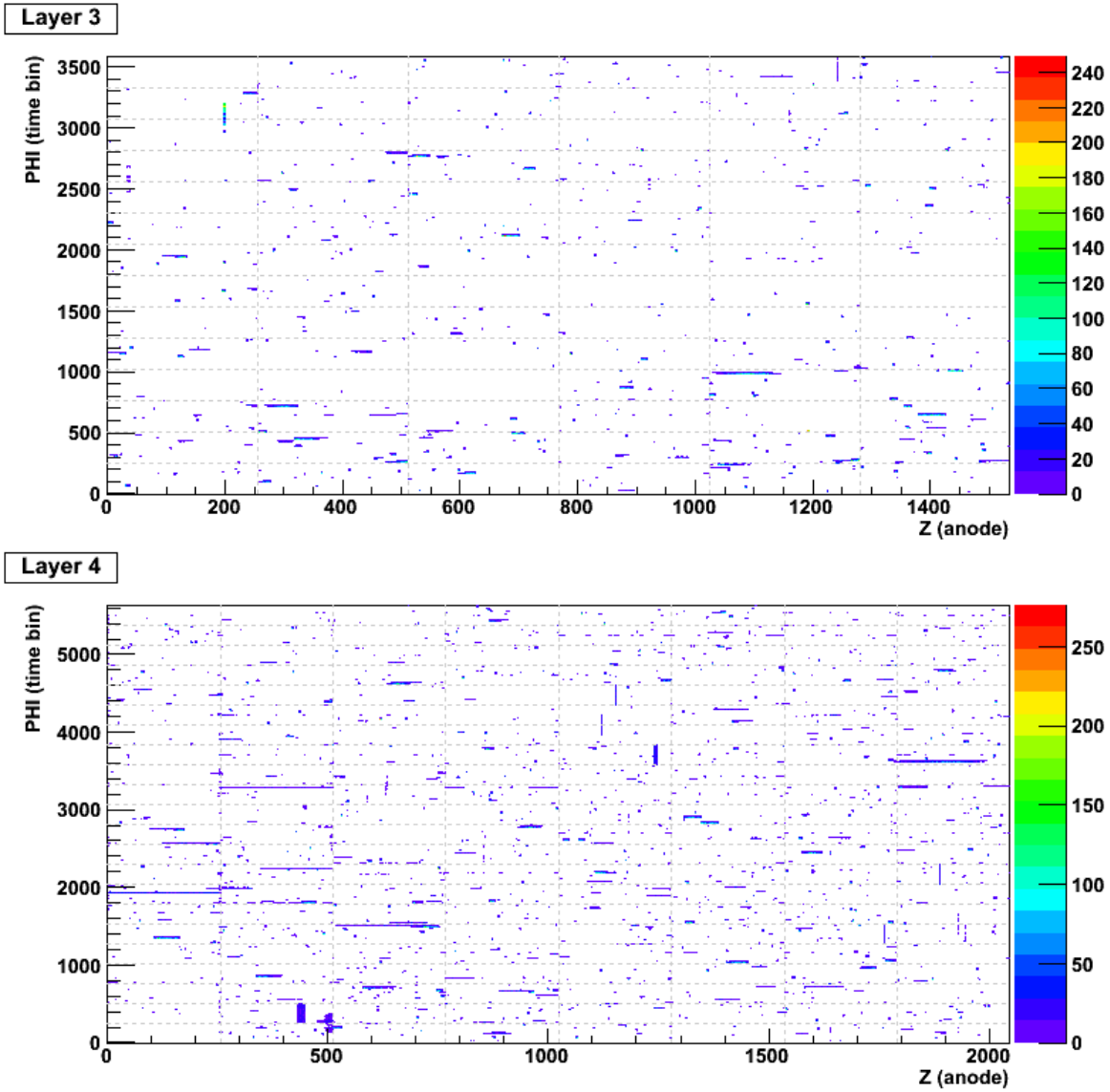
Esempi di tracce



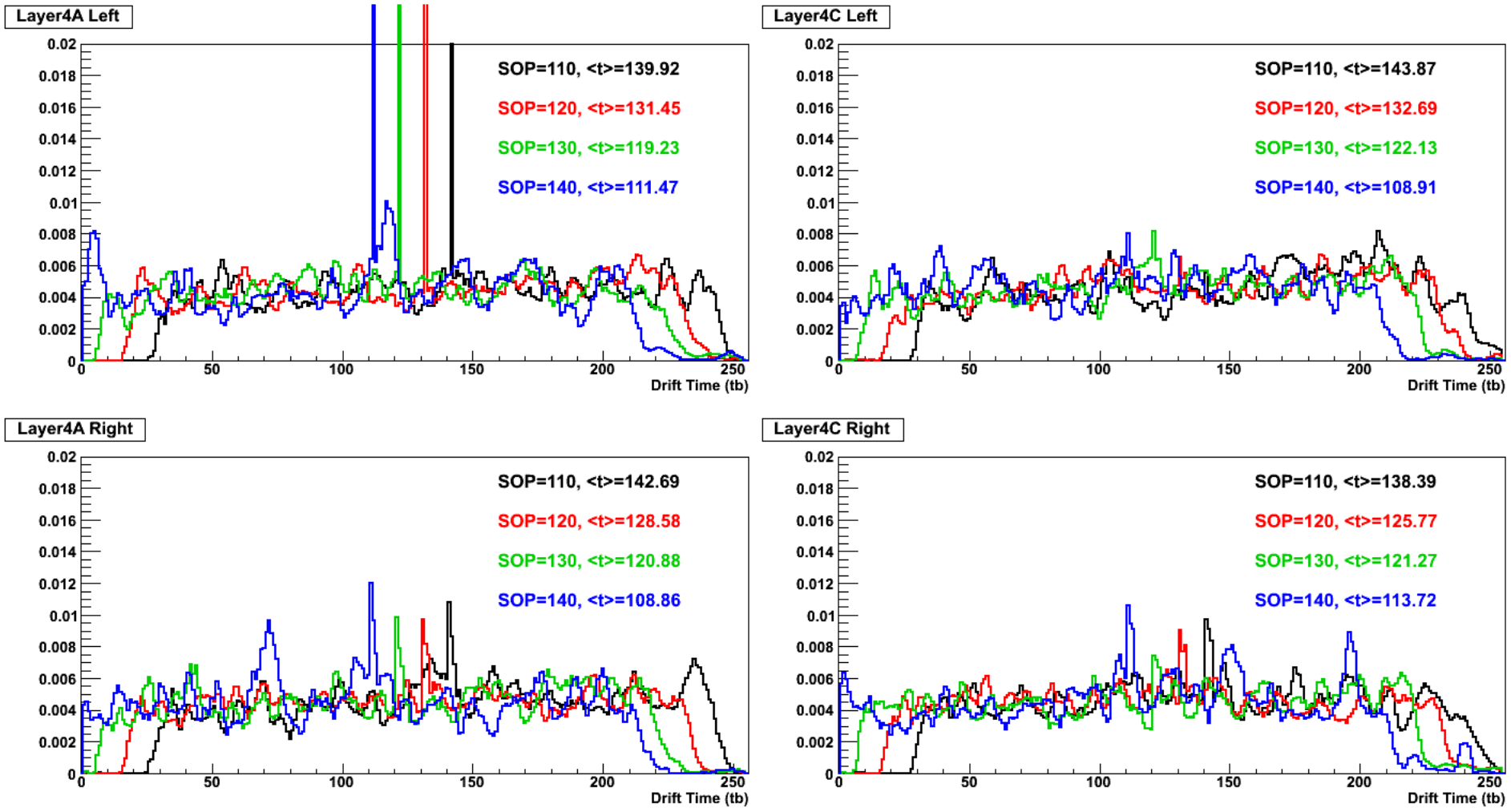




Event display di SDD durante un test di iniezione (12/7/2009)



Ottimizzazione del SOP delay



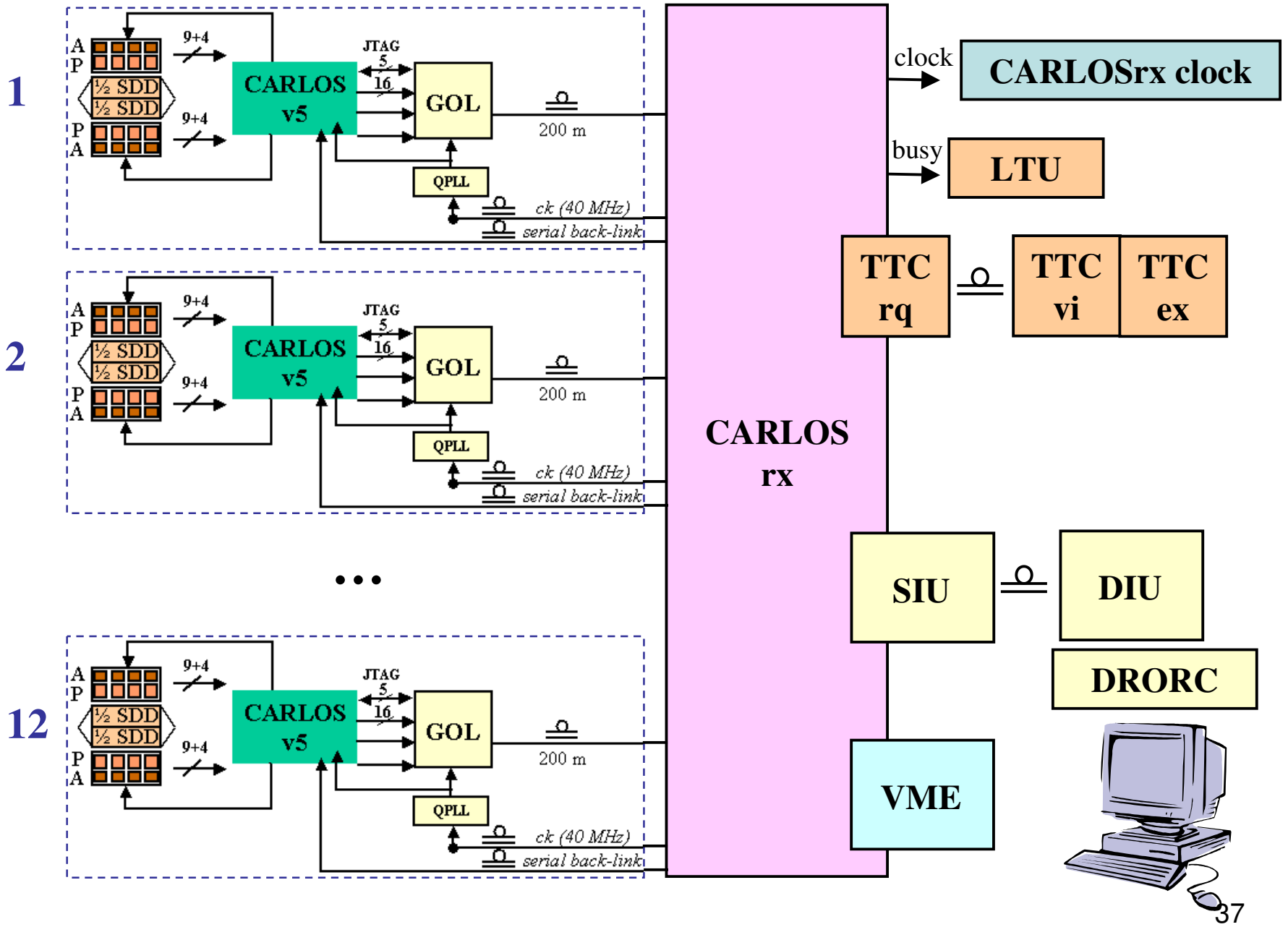
Il valore ottimale del SOP delay è **125**

Conclusioni

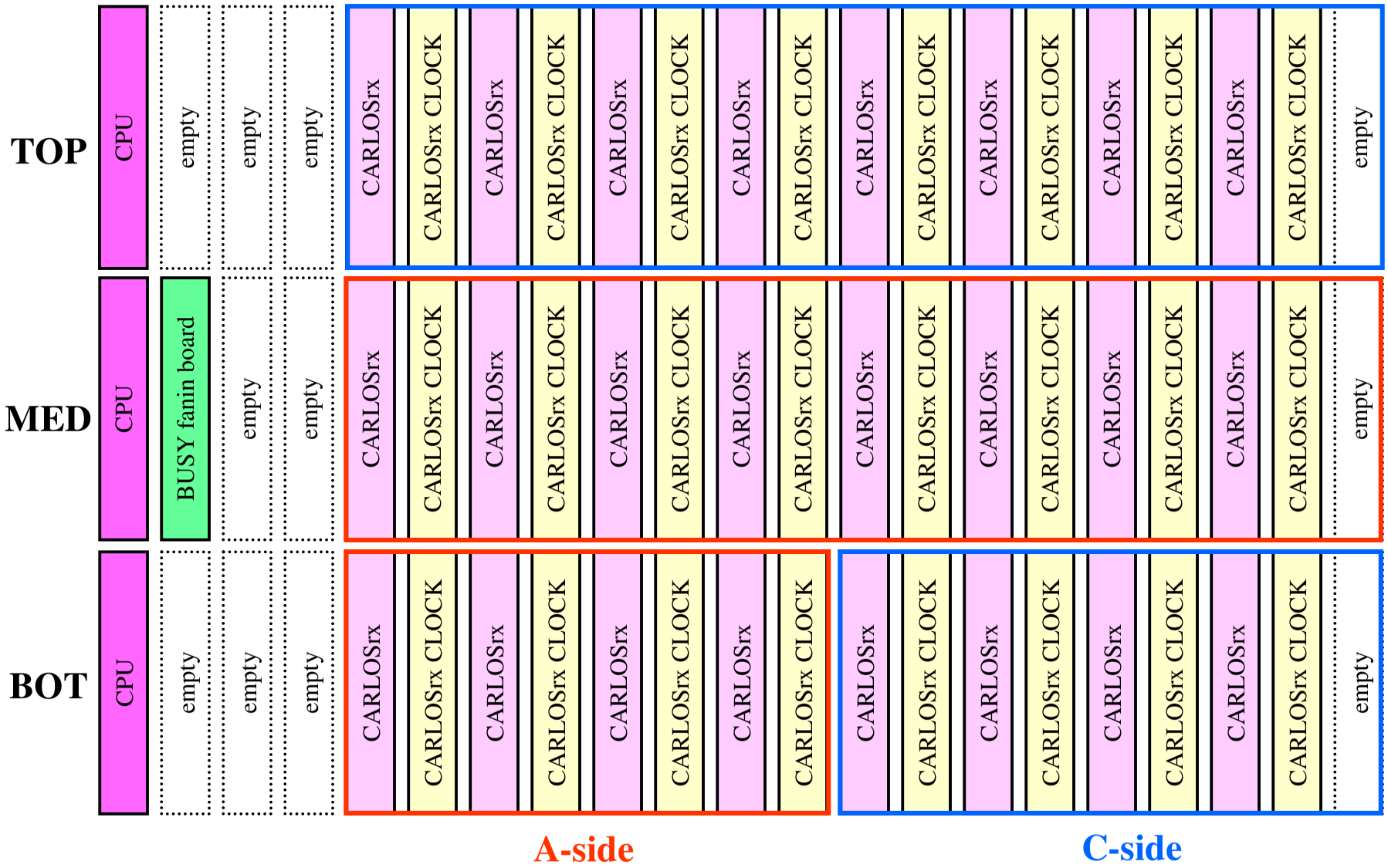
- Il funzionamento del detector è soddisfacente e le calibrazioni sono sotto controllo.

- Vedi anche i seguenti talk:
  - ⇨ Test per la validazione dell'allineamento dell'ITS, Andrea Rossi (TS)
  - ⇨ Identificazione di particelle nell'ITS, Emanuele Biolcati (TO)

Backup slides


1
2
12
A P
½ SDD
½ SDD
P A
9+4
9+4
CARLOS v5
JTAG
5
16
GOL
200 m
QPLL
ck (40 MHz)
serial back-link
CARLOS rx
clock
CARLOSrx clock
busy
LTU
TTC rq
TTC vi
TTC ex
SIU
DIU
DRORC
VME

3 readout VME crates in CR4 (CARLOSrx)



Dump of an event with 2D compression

CDH

end of module + jitter

```
.....................................................................
Size:940 (header:68) Version:0x00030009 Type:PhysicsEvent
RunNb:1010 Period:0 Orbit:14113515 BunchCrossing:2880 ldcId:1 gdcId:VOID
time:Mon Feb  9 14:38:30 2009
Attributes:0+1+2+3+4+5+6+7+Orbit/BC(000000ff.00000000.00000020)
triggerPattern:80000000-00000001 detectorPattern:80000004=(2=SSD-HW)
  0) 00000368 00000011 00000100 00000000          | h... .... .... .... |
 16) 00000000 00000000 00000004 ffffffff          | .... .... .... .... |
 32) 02050b40 00d75aeb ff000000 00000b62          | @... .Z.. .... b... |
 48) 00000001 00000000 00000000 fffffff           | .... .... .... .... |
 64) 2000bd5e 2000c28e 2008bd5e 2008c296          | ^..  ...  ^..  ...  |
 80) 2010bd5e 2010c29e 2020bd5e 2020c29e          | ^..  ...  ^.   ..   |
 96) 2028bd5e 2028c29e 2030bd5e 2030c29e          | ^.(  ..(  ^.0  ..0  |
112) 2040bd56 2040c29e 2048bd5e 2048c29e          | V.@  ..@  ^.H  ..H  |
                              ...
800) 23d0bd66 23d0c25e 23e0bd66 23e0c256          | f..# ^..# f..# V..# |
816) 23e8bd66 23e8c256 23f0bd66 23f0c256          | f..# V..# f..# V..# |
832) fffffff4 fffffff6 fffffff9 fffffffa          | .... .... .... .... |
848) fffffff0 fffffff1 fffffff2 fffffff7          | .... .... .... .... |
864) fffffff8 8f000006                            | .... .... |
```

Performances
(256 samples x anode, AM & ADC 40 MHz, VREF CTRL DAC = 70, CARLOS thresholds= 0)

	Event size (MByte)	Max rate (Hz)
1 module	0.5	193
2 modules	1	144
4 modules	2	76
6 modules	2.8	54
8 modules	3.9	40
10 modules	5	32

Performances
(256 samples x anode, AM & ADC 40 MHz, VREF CTRL DAC = 70, CARLOS thresholds= 0xFF)

	Event size (Byte)	Max rate (Hz)
1 modulo	140	500
2 moduli	144	500
4 moduli	152	500
6 moduli	160	500
8 moduli	168	500
10 moduli	176	500
12 moduli	184	500

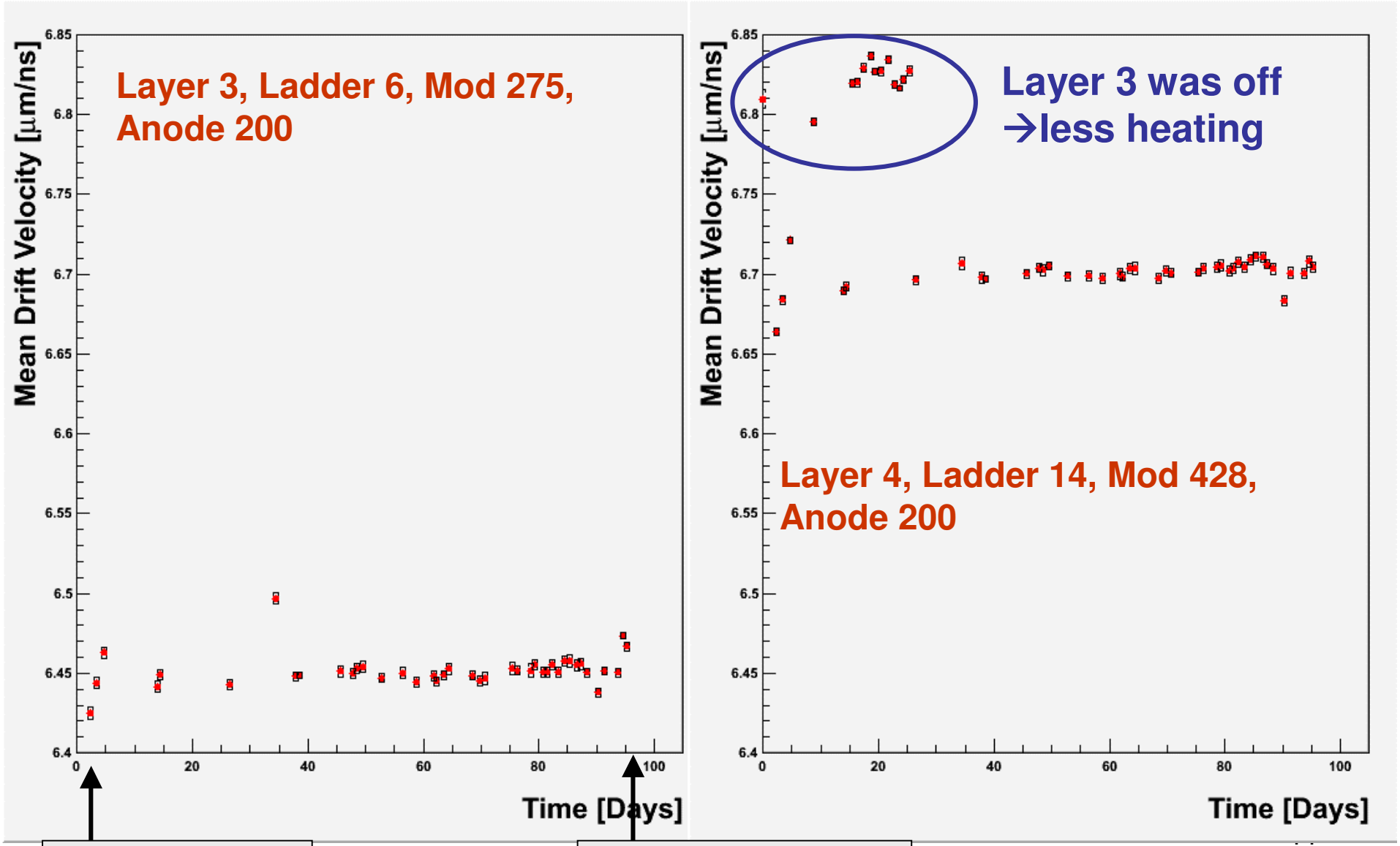
Performances with testpulse
(256 samples x anode, AM & ADC 40 MHz,
VREF CTRL DAC = 70, CARLOS thresholds= 0x50)

	Event size (KBytes)	Max rate (Hz)
1 module	2.3	500
2 modules	3.4	500
4 modules	6.5	500
6 modules	17	500
8 modules	22	500
10 modules	28.7	500

Performances with testpulse
(128 samples x anode, AM @ 20 MHz, ADC @ 40 MHz, VREF CTRL DAC = 70, CARLOS thresholds= 0x50)

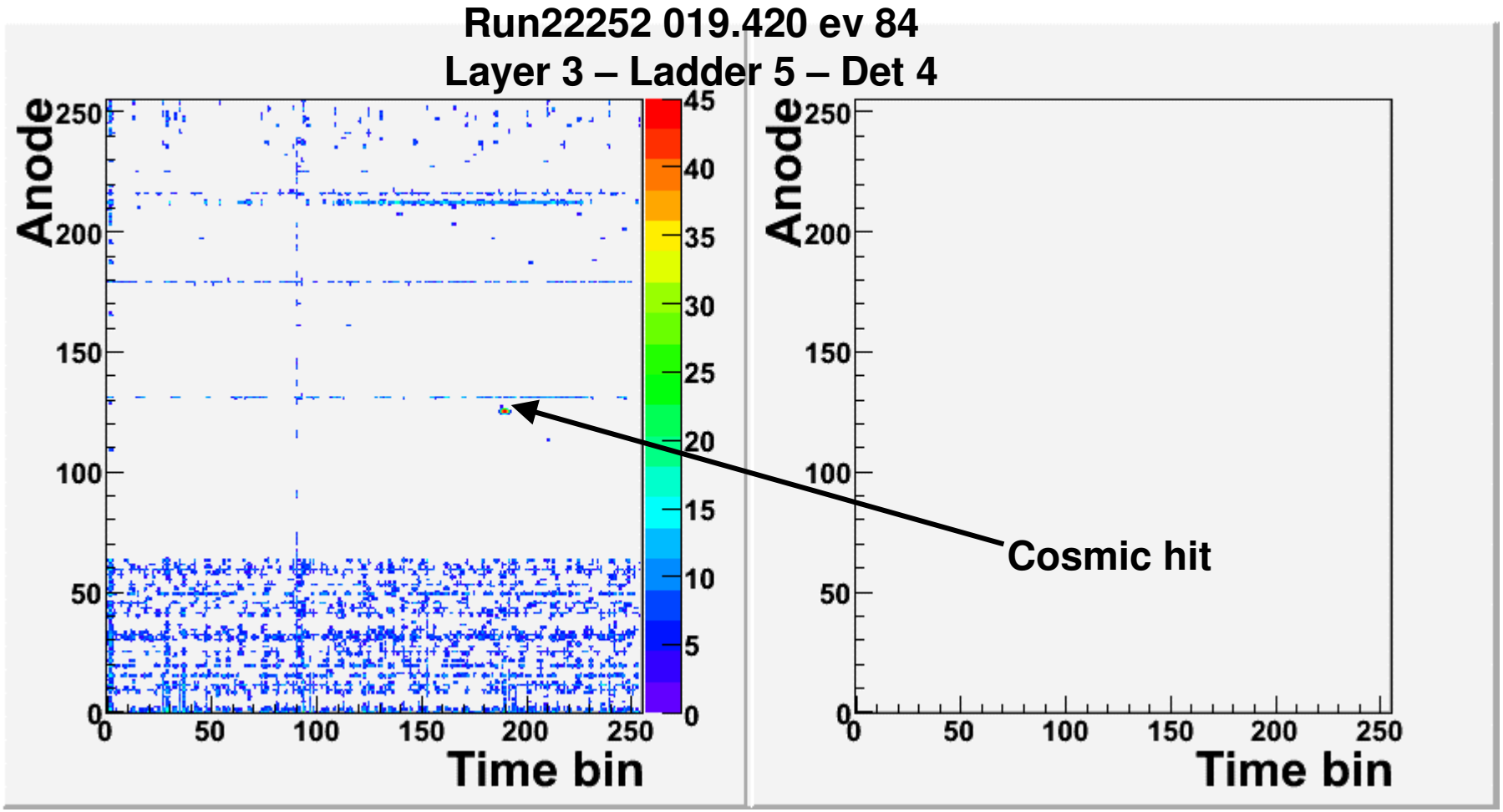
	Event size (KByte)	Max rate (Hz)
1 module	2.6	990
2 modules	4.6	990
4 modules	10	990
6 modules	13	990
8 modules	19.5	990
10 modules	24.8	990

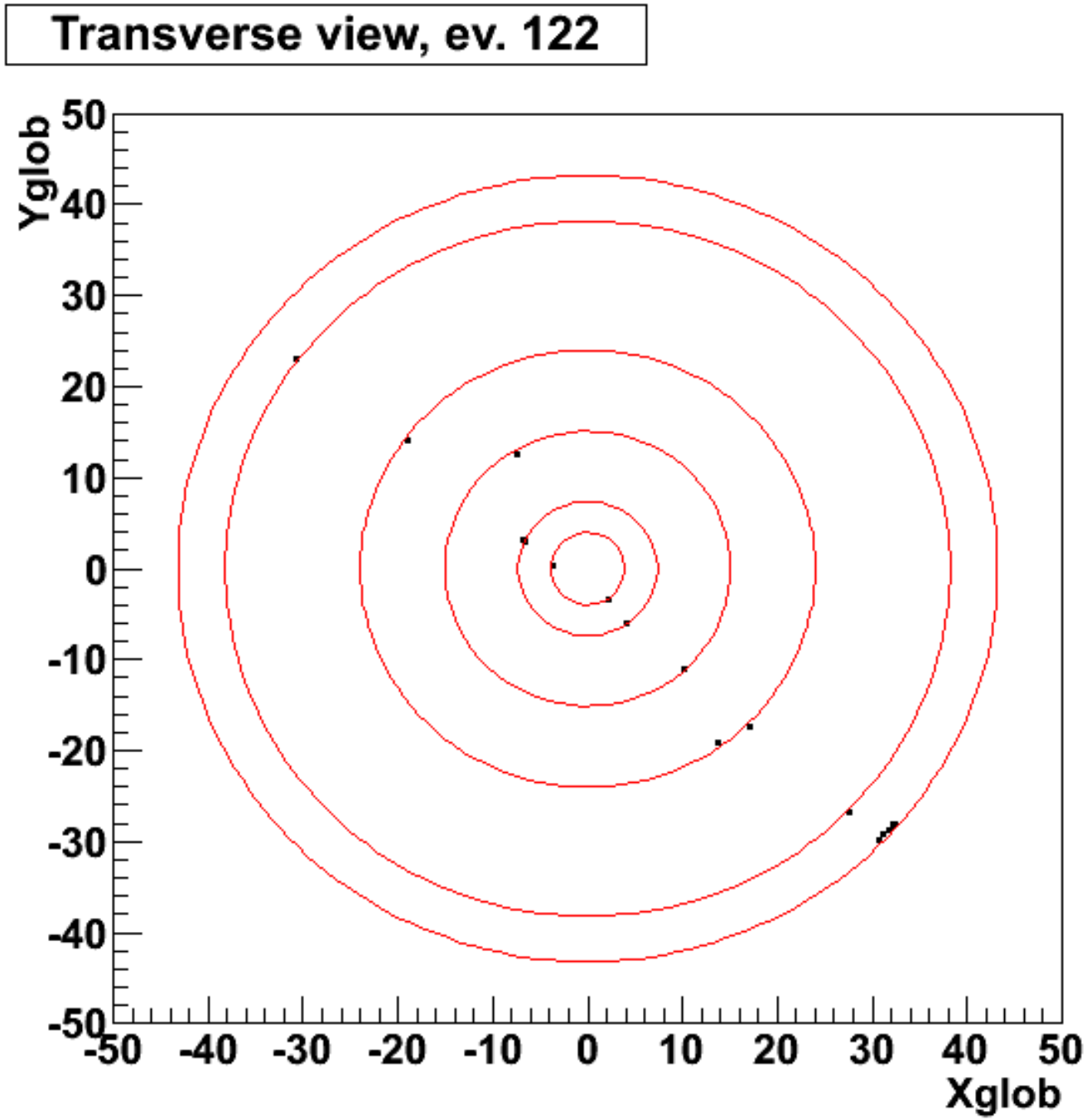
Drift speed vs. time

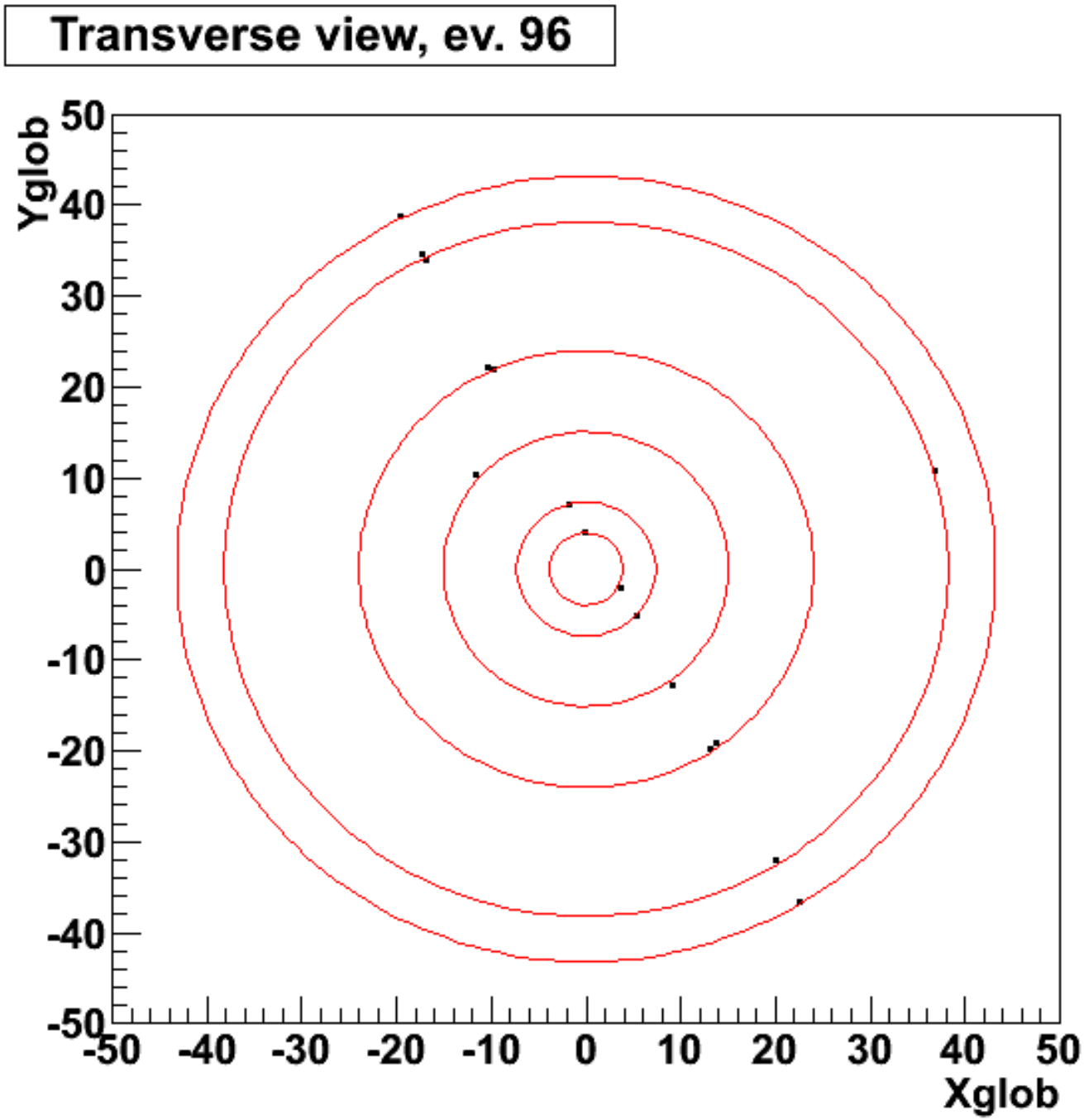


SDD hit

- Esempio di modulo con anodi rumorosi




Transverse view, ev. 122
Yglob
Xglob
50
40
30
20
10
0
-10
-20
-30
-40
-50
-50
-40
-30
-20
-10
0
10
20
30
40
50


Transverse view, ev. 96
Yglob
Xglob
50
40
30
20
10
0
-10
-20
-30
-40
-50
-50
-40
-30
-20
-10
0
10
20
30
40
50